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A MODULE EXPERIMENTAL PROCESS SYSTEM  
DEVELOPMENT UNIT (MEPSDU)

Quarterly Report No. 1

November 26, 1980 to February 28, 1981

Contract No. 955902



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The JPL Low-Cost Solar Array Project is sponsored by the U.S. Department of Energy and forms part of the Solar Photovoltaic Conversion Program to initial a major effort toward the development of low-cost solar arrays. This work was performed for the Jet Propulsion Laboratory, California Insitute of Technology by agreement between NASA and DOE.

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## ABSTRACT

The purpose of this program is to demonstrate the technical readiness of a cost-effective process sequence that has the potential for the production of flat plate photovoltaic modules which met the price goal in 1986 of 70¢ or less per Watt peak.

During this initial program quarter, the efforts have included preparation and submission of the Work Breakdown Structure, the Baseline Cost Estimate and the Program Plan. The proposed process sequence was reviewed and laboratory verification experiments were conducted. The preliminary process includes the following features:

- Semicrystalline silicon (10cm x 10cm) as the silicon input material.
- Spray-on dopant diffusion source.
- Al paste BSF formation.
- Spray-on AR coating.
- Electroless Ni plate-solder dip Metallization.
- Laser scribe edges.
- K & S tabbing and stringing machine.
- Laminated EVA modules.

## QUARTERLY REPORT

### TABLE OF CONTENTS

	<u>Page</u>
1.0 Introduction	1
2.0 Process Description	6
2.1 Input Material	6
2.2 Detailed Cell Process Description	7
2.3 Detailed Module Design	20
2.4 Tabbing and Stringing Machine Design	29
2.5 Module Encapsulation	50
2.6 Test System	53
2.7 QA Plan	62
2.8 Preliminary Cost Estimate	65
3.0 Technical Progress	67
3.1 Documentation	67
3.2 Kulicke and Soffa Industries, Inc. Subcontract	67
3.3 Surface Preparation	68
3.4 Front Junction Formation	69
3.5 Back Junction Formation	73
3.6 AR Coating	75
3.7 Metallization	76
3.8 Edging	81
3.9 Cell Design	82
3.10 Module Design	89
3.11 Tabbing and String Machine	93
3.12 Module Encapsulation	97
4.0 Recommendations and Schedule	105
References	107

## LIST OF FIGURES

	<u>Page</u>
1. General Process Sequence	4
2. Surface Preparation Process Sequence	8
3. Front Junction Process Sequence	10
4. Back Junction Process Sequence	12
5. AR Coating and Grid Pattern Definition Process Sequence	14
6. Metallization Process Sequence	16
7. Edging Process Sequence	19
8. Module Lay-out	21
9. Module Cross-Section	22
10. AMP Connector	26
11. Interconnect	28
12. Flow Diagram of Tapping and Stringing Machine	30
13. K&S Automated Tapping and Stringing Machine	31
14. Unload and Alignment Station	34
15. Walking Beam Conveyor	35
16. Insulating Tape Application Station	37
17. First Flux Application Station	38
18. First Interconnect Stations	39
19. Cell Inverter Station	40
20. Interconnect Foldover Station	42
21. Cell Transfer Station	43
22. String Conveyor	44
23. Second Flux Application Station	46
24. Second Stringing Interconnect Station	47
25. String Pickup and Transfer Station	48
26. Module Encapsulation Process Sequence	51
27. Cell Test Process Sequence	54
28. Block Diagram of Cell Test System	55
29. Cell Test Subsystem Components and Data Flow	56
30. Cell Measurement Overview Flowchart	57
31. Module Test System Process Sequence	58
32. Module Test Subsystem Component and Data Flow	60

	<u>Page</u>
33. Module Test Overview Flowchart	61
34. MEPSDU Cell Outline and Pad Placement	83
35. MEPSDU Grid Pattern	88
36. MEPSDU Top Assembly	90
37. MEPSDU Cell Assembly	91
38. MEPSDU Electrical Schematic	92
39. Interconnect Configuration	94
40. Linear Low Density Polyethylene Data Sheet	98
41. ODR Test at 150°C	100
42. ODR Test at 140°C	101



## 1.0 Introduction

The purpose of the MEPSDU program is to demonstrate the technical readiness of a cost-effective process sequence that has the potential to produce flat-plate photovoltaic modules which meet the 1986 pricegoal of less than \$.70 per peak Watt. To achieve their goal, Solarex will design, develop and fabricate a Module Experimental Process System Development Unit (MEPSDU) and will utilize the unit to produce a quantity of modules using the proposed process sequence. This effort will include:

- Design of a detailed cost effective process sequence,
- Completion of a detail design of the MEPSDU,
- Fabrication and assembly of the MEPSDU,
- Preparation of a process instruction manual, including in-line process control information,
- Performance of a minimum of three technical demonstrations which will include the production of sufficient modules and production data to permit validation of the contract goal,
- Performance of a cost analysis of the process sequence, including a study of the cost impact and changes required in the MEPSDU to allow the use of different types of input material.

In selecting a process sequence, we have emphasized the following considerations:

- Economics,
- State of verification,
- Availability of equipment for automation,
- Ease of integrating individual processes,
- Compatibility with the selected input material and a variety of other alternative silicon sheet materials.

In our design of the MEPSDU, we have chosen to develop a unit that is a forerunner of a production facility. This means that we will utilize production equipment, not laboratory-scale equipment. All manual handling of individual cells will be eliminated.

The concept of the MEPSDU is to demonstrate the process sequence and machinery by utilizing a single, rather than several parallel machines for each station. This means that the line itself is not a balanced production line, but all of the throughput rates are sufficient to demonstrate automated manufacture. Indeed, this unit itself will be capable of producing close to 10 MW per year with only minor modification (e.g. addition of several more laminating stations).

The general process sequence is shown in block form in Figure 1. The incoming sheet material we have chosen is cast semicrystalline silicon in the form of 10 cm x 10 cm wafers. The process includes spray-on dopant with belt diffusion, Al paste BSF spray-on AR coating, electroless Ni plating with solder dipping, laser scribing and lamination with a glass superstrate. The details of the process sequence and the module design is given in Section 2.

Results of experiments performed in the first quarter are presented in Section 3. Section 4 summarizes our progress to date, including recommendations and conclusions, as well as presenting a brief schedule for the next quarter.

Figure 1

GENERAL PROCESS  
DESCRIPTION

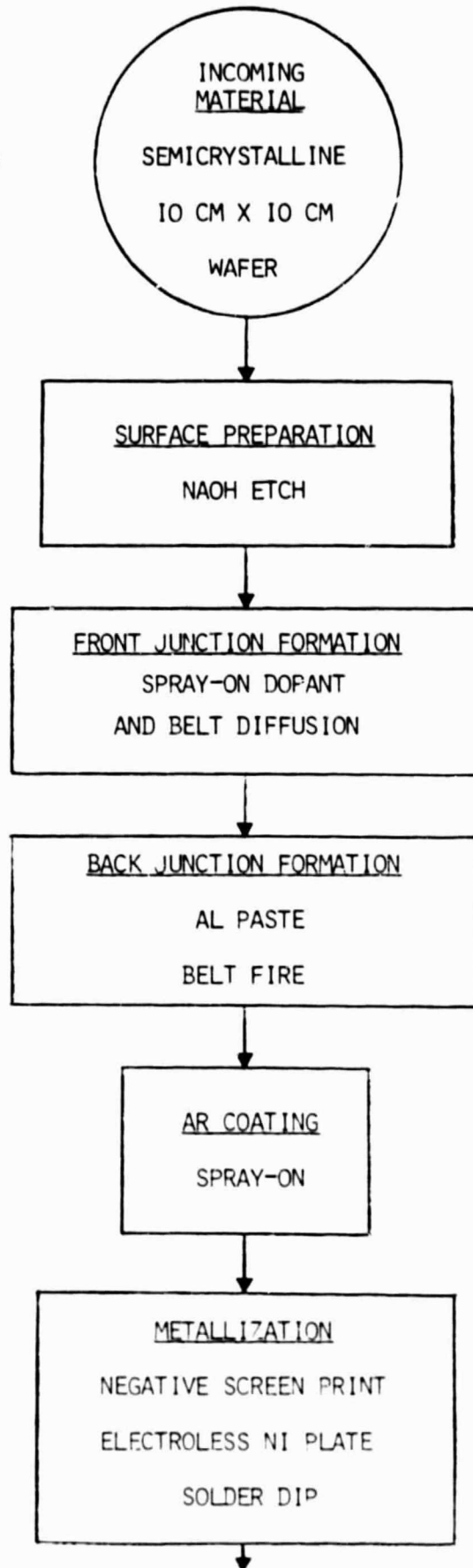
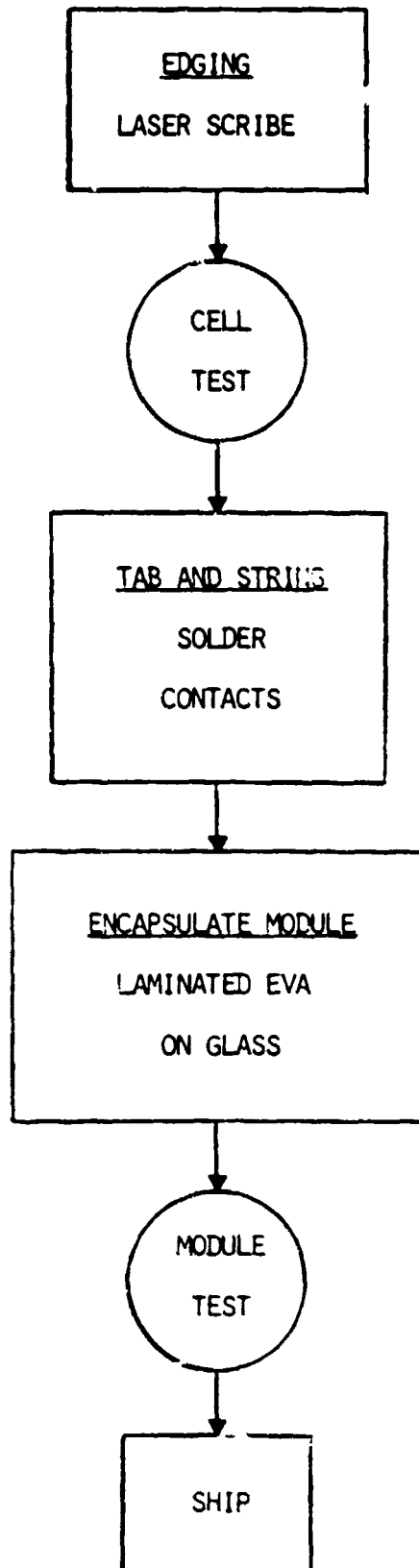


Figure 1 (cont'd)



## 2.0 Process Description

### 2.1 Input Material

Semicrystalline 10 cm x 10 cm wafers were chosen as the input material for our MEPSDU because:

- The material is available for use now.
- It is closely related to other advanced sheet materials presently in the development stage.
- Analyses indicate that it can be produced for a cost within the \$.70/Watt goal. Wafer costs as low as 30.6¢/Watt (reference 1) have been calculated.
- Solarex has sufficient experience with the processing of this material to understand its behavior through the various process steps.

The semicrystalline wafers will be p-type silicon with a resistivity between 0.5 and 10  $\Omega$ -cm. The wafers will have a thickness varying from .012 in. to 0.016 cm. The corners will be cropped to reduce breakage and allow for improved automatic handling.

## 2.2 Detailed Cell Process Description

### 2.2.1 Surface Preparation

Work damage is removed from the wafers by etching in a solution of sodium hydroxide. Texturing and grain boundary steps can be minimized by using a high concentration (30% by weight NaOH in water), high temperature (120°C) and short etch times (approximately two minutes). Due to high activity of the etch, a precleaning step is not necessary.

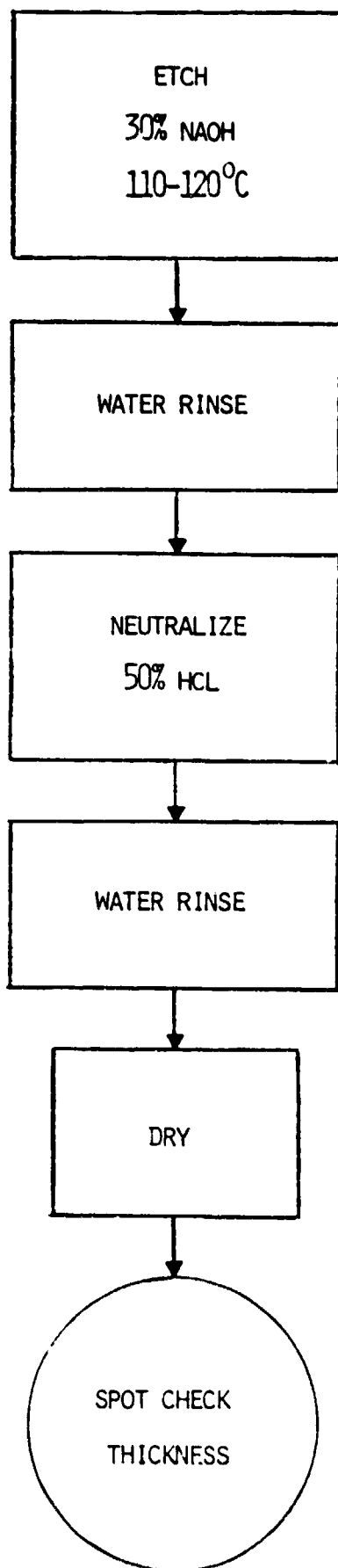
The process sequence for surface preparation is shown in Figure 2. After the etch itself, the wafers are rinsed in water, neutralized with hydrochlorine acid (HCl:H<sub>2</sub>O, 1:1), rinsed in deionized water and dried.

Sodium hydroxide etching was chosen mainly on the basis of economy. The alternates investigated were:

- Acid etching, which has too high a materials cost, and
- Plasma etching, which has too high a capital equipment cost.

Sodium hydroxide etching is utilized extensively in production at Solarex. In addition, it has been verified by a number of contractors, including Solarex (2), Sensor Technology (3) and Lockheed (4). Our preliminary cost estimate for this process

Figure 2  
SURFACE PREPARATION





(based on the IPEG approximation) is \$0.0075 per Watt. The details of these analyses are given in Table 1.

### 2.2.2 Front Junction Formation

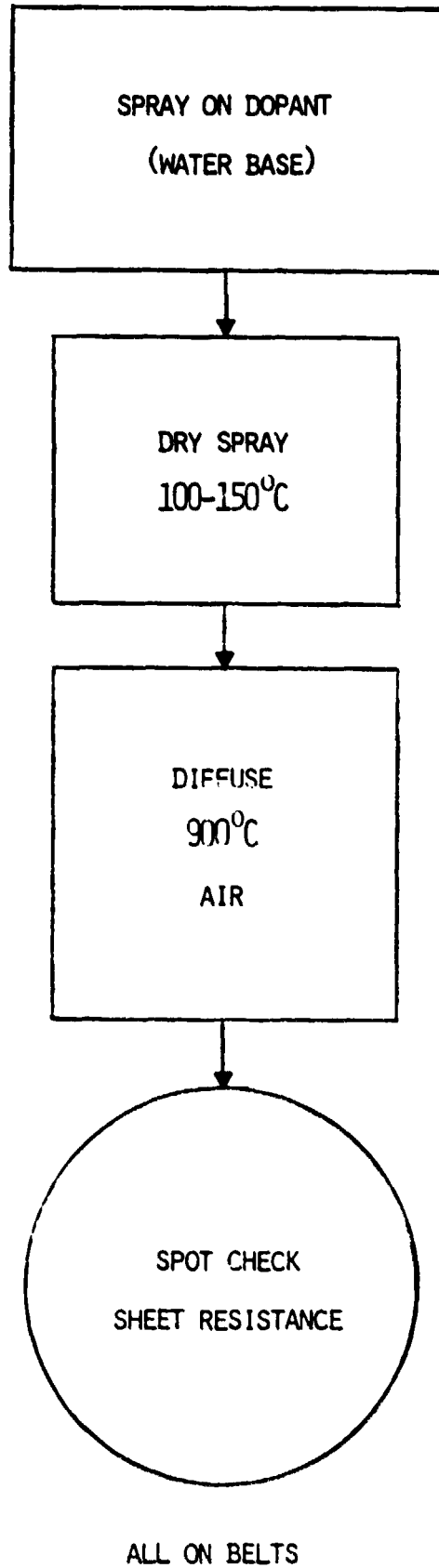
A water base solution (phosphorosilica film), available commercially from Emulsitone Corporation, has been formulated specially for spray-on application in the processing of solar cells. The process sequence is shown in Figure 3. Once the wafers are sprayed, they are dried at a low temperature (100-150°C) for about 12 minutes. Diffusion is performed in a belt furnace at 900-905°C for 10 minutes in an air ambient, resulting in a sheet resistance of approximately 40  $\Omega/\square$ .

Spray-on and spin-on diffusion has been verified by Spectrolab (5), Sensor Technology (6) and the manufacturer. The resultant diffusion oxides are readily removed as long as the diffusion is performed in the presence of oxygen. Belt diffusion has been verified by Solarex (7) and is used on a daily basis at Solarex.

The alternative front junction processes studied were:

- Gaseous diffusion, which is somewhat more expensive and requires extensive equipment clean-up without any performance advantages,
- Ion implementation, which requires expensive equipment without any performance advantages.

Figure 3  
FRONT JUNCTION FORMATION



Our preliminary cost estimate for this process is \$0.014/Watt.

### 2.2.3 Back Junction Formation

We have chosen to utilize screen-printed aluminum paste for BSF formation. Figure 4 shows the process sequence. A layer of Englehard A3484 aluminum paste is screened onto the back of the wafer. The wafers are then transferred to a belt furnace where the paste is first dried at a low temperature (150 to 250°C) and then fired at a high temperature (850°C) for a short time (less than one minute).

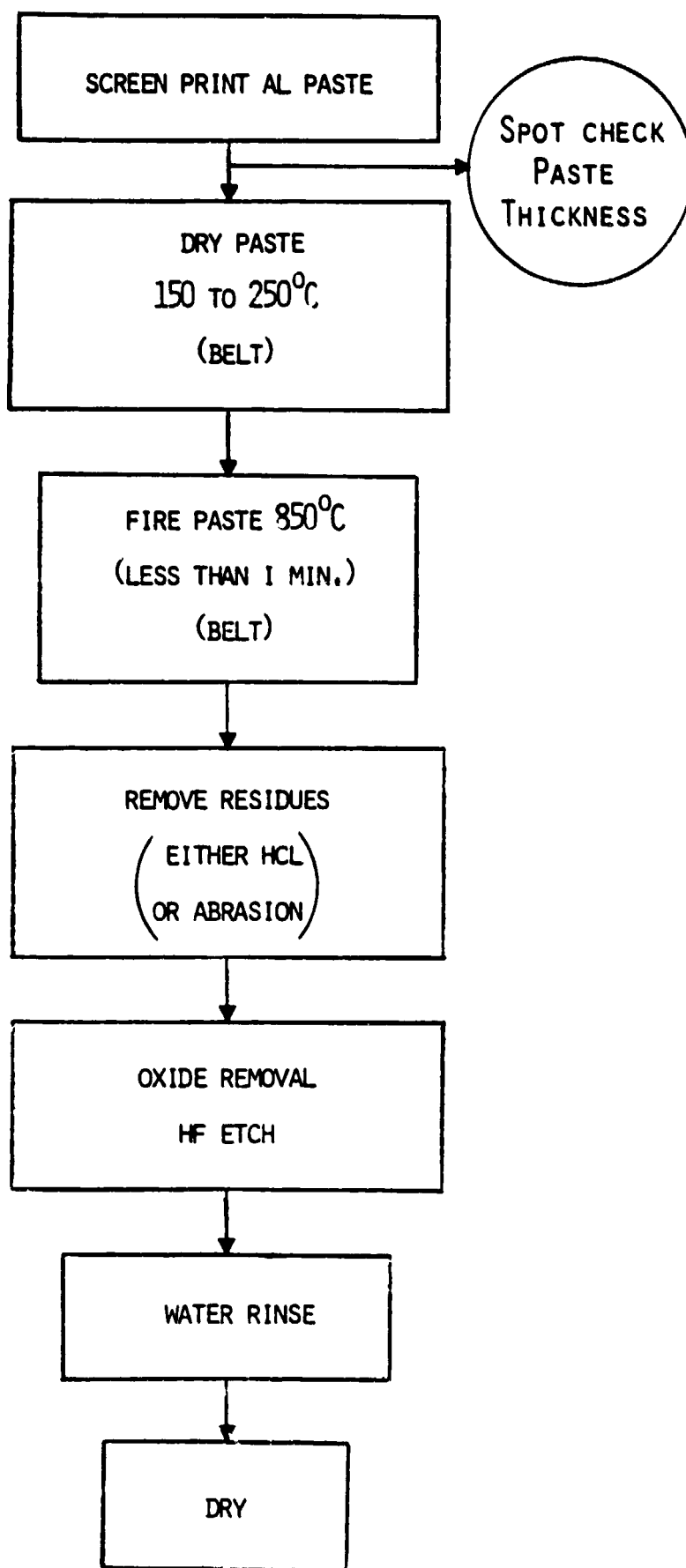
We are still investigating two possible back clean-up processes. The first one entails an etch in hot HCl to remove the unalloyed Al. The second alternative is to sand blast the back with glass beads to remove the charred residue but to leave most of the Al to serve as a current carrying media.

After back clean-up, the wafers are etched in HF to remove oxides from both sides of the wafer. Finally, the wafers are rinsed and dried.

The Al paste BSF process was chosen because:

- It is consistent with the production of high-efficiency solar cells (8,9).
- It is tolerant of variations in the incoming silicon resistivity.

Figure 4  
BACK JUNCTION  
FORMATION



- The required equipment is available and is consistent with volume processing.
- It is utilized extensively in production at Solarex.

Our preliminary cost estimate for the proposed BSF process step is \$0.026/Watt.

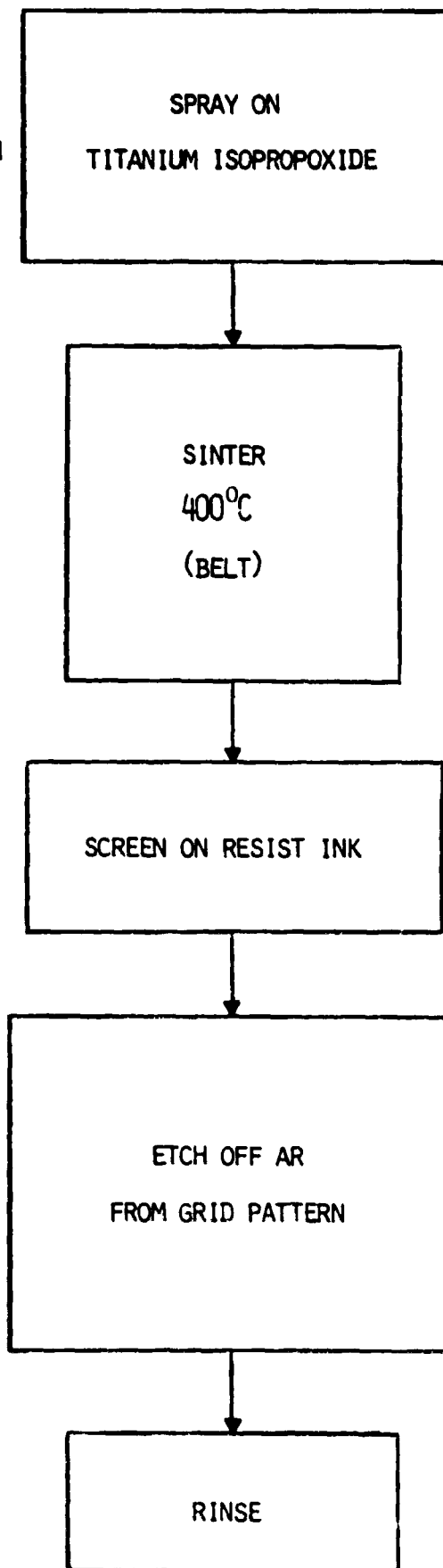
#### 2.2.4 AR Coating and Grid Pattern Definition

We have selected a spray-on technique for applying the AR coating. The process sequence is shown in Figure 5. The wafers are sprayed with a titanium isopropoxide solution and transferred to a belt where the solution is dried at 125°C and then sintered at 450°C. The wafers then have a resist screened on, leaving the area to be metallized uncovered. The resist is cured with a 100°C bake for from 10 to 20 minutes. The AR coating is then removed from the pattern by etching in the fumes created by Fumic HF. Finally, the wafers are rinsed in deionized water.

We have chosen to apply the AR coating before metallization because it simplifies the spraying process, protects the areas of the silicon surface that are not metallized, and can be sintered at high temperature without danger of metal penetration through the junction.

Other AR coating techniques evaluated were:

Figure 5  
AR COATING  
AND  
GRID PATTERN



- Vacuum evaporation, which requires high capital equipment costs and has a low throughput,
- Spin-on, which is not well suited to large square wafers,
- Dipping, which is better suited for long, narrow cells, and
- CUD, which has high capital equipment costs and a low throughput.

Our estimate for the cost of the AR coating is \$0.0093/Watt.

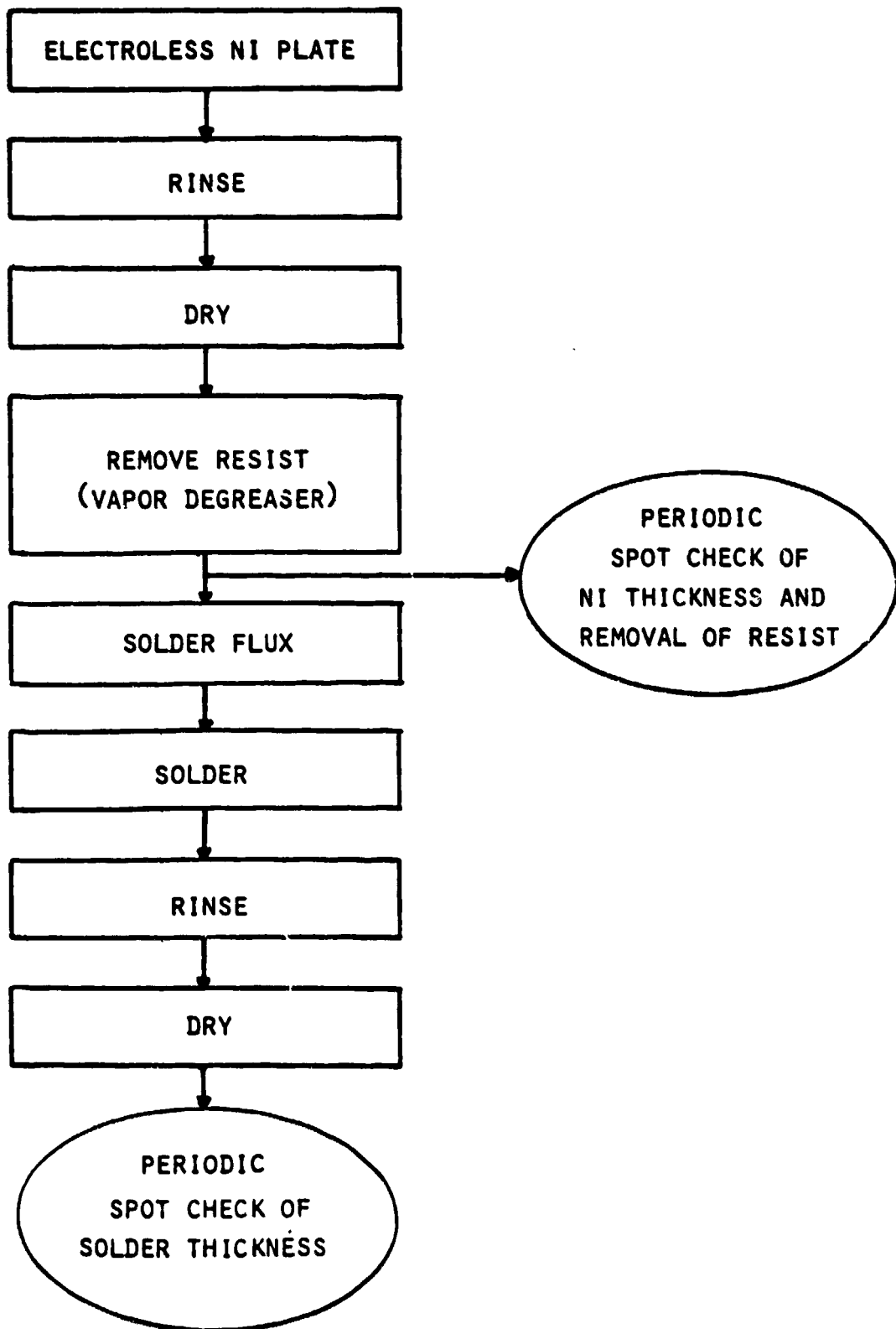
Screen printing was chosen because it is compatible with electroless nickel plating and with the available equipment. Our estimate for the cost of screen printing the resist pattern is \$0.0168/Watt.

#### 2.2.5 Metallization

Solarex has selected an electroless nickel-solder contact system. The process sequence is shown in Figure 6. The cells go directly from the water rinse into the Halma electroless nickel plating bath for seven minutes. The cells are then rinsed and dried. The resist is removed from the cell by an organic solvent (probably trichloroethane). The cells are then fluxed, wave soldered, rinsed and dried. If the second back clean-up option is utilized, only the front of the cell

Figure 6

## METALLIZATION





will be wave soldered, since the Al-Ni on the back is sufficient both to carry the current and for solderability of the contacts.

A number of alternate metallization techniques were considered, including:

- Screen-printed contacts - These systems suffer from high cost of materials (silver), lower conductivity of the screen-printed material and their limited thickness.
- Copper plating - There is insufficient evidence that copper can withstand the environmental stresses.
- Aluminum - This system has not been verified and a cost effective deposition technique has not been identified.
- Alternate Ni-solder systems - More complicated (and expensive) techniques have been proposed, but our experiments (10) indicate that these techniques have no advantage over the simple system proposed here.

The estimated cost for etching out the AR coating, doing the Ni plating and removing the resist ink is \$0.0219/Watt. The estimated cost for wave soldering of one side only is \$0.0234/Watt.

### 2.2.6 Edging

Solarex has elected to use a laser scribing system for etching. The process sequence is shown in Figure 7. The cells are unloaded from cassettes scribed and reloaded into cassettes. The scribed line width is about 0.001 in. with a depth penetration of 0.001 in. It is still to be determined whether the laser scribing system will scribe a pattern or if it will be an edge follower system. The distance between the edge and the laser scribe will be a minimum of 0.010 in.

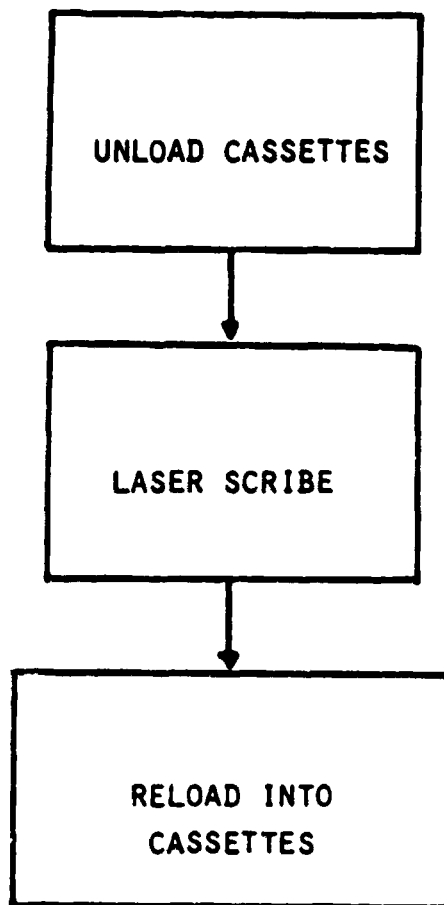
The alternatives considered for edging are:

- Mechanical abrasion, which tends to produce damaged areas that serve as shunting paths or as sources for future breakage,
- Etching, which requires complicated and expensive masking of the junction.

Laser scribing has been verified by Sensor Technology (6,11,12).

The preliminary cost estimate for laser scribing (based on a pattern scribe) results in a cost of \$0.014/Watt.

Figure 7  
EDGING



### 2.3 Detailed Module Design

The preliminary module design calls for utilizing 72 10 cm. x 10 cm. semicrystalline cells with an electrical hook-up of 2 cells in parallel with 36 series blocks. The module will be approximately 66 cm. x 126 cm. or 26 in. x 49.6 in. We believe that this size is large enough for economic production but small enough to be able to handle both in production and during installation. Figure 8 shows the preliminary module lay-out. Cell paralleling and the use of three internal bypass diodes are designed to protect the module from hot spot problems.

The module cross-section is shown in Figure 9. The components are described below.

A glass superstrate has been selected because it:

- Filters out UV,
- Withstands oxidants, stains, etc.,
- Withstands the effects of rain, wind and hail,
- Is readily cleanable,
- Serves as both a protective cover and structural support,
- Is utilized extensively in the photovoltaic industry,

Figure 8  
Module Lay-Out

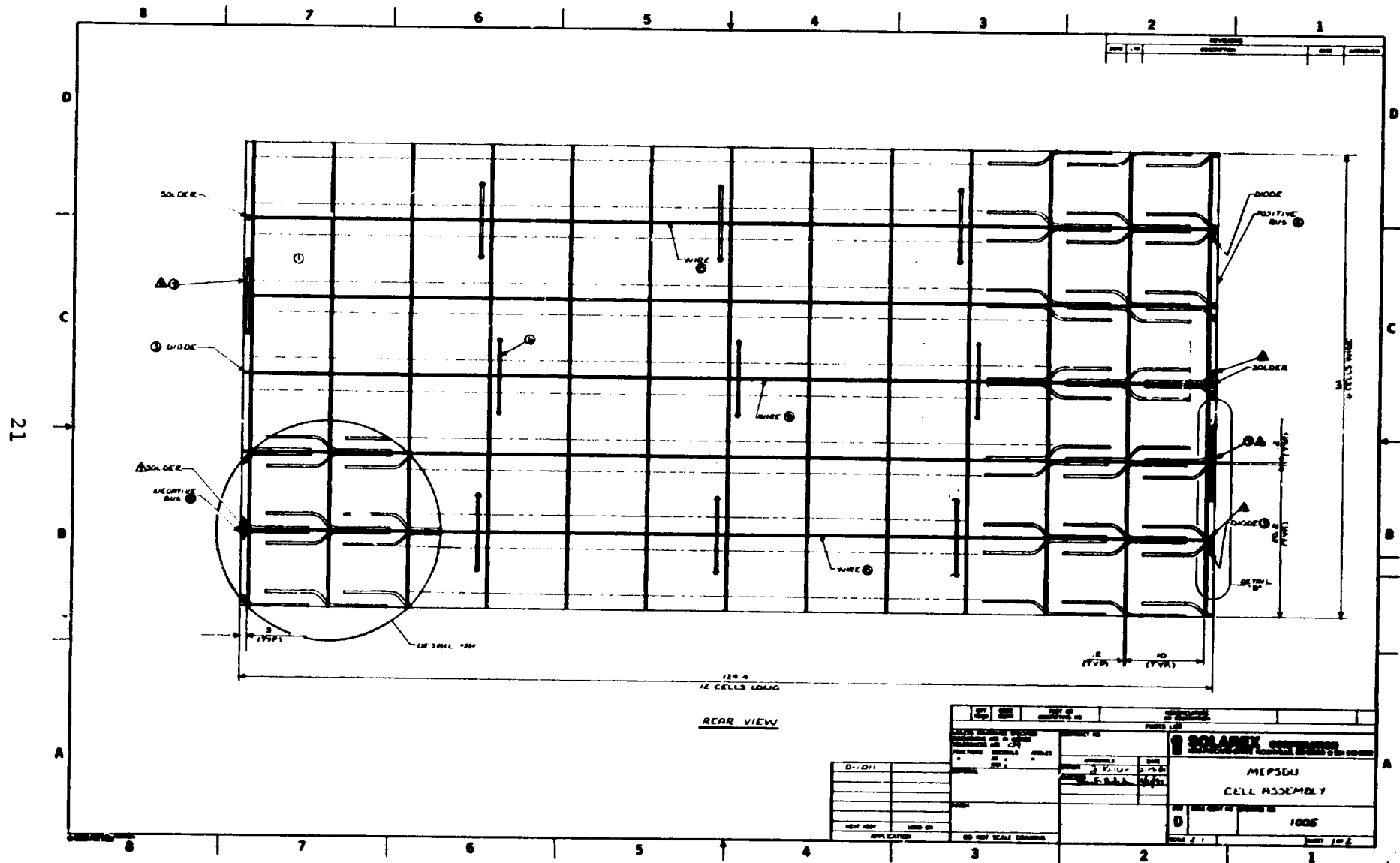
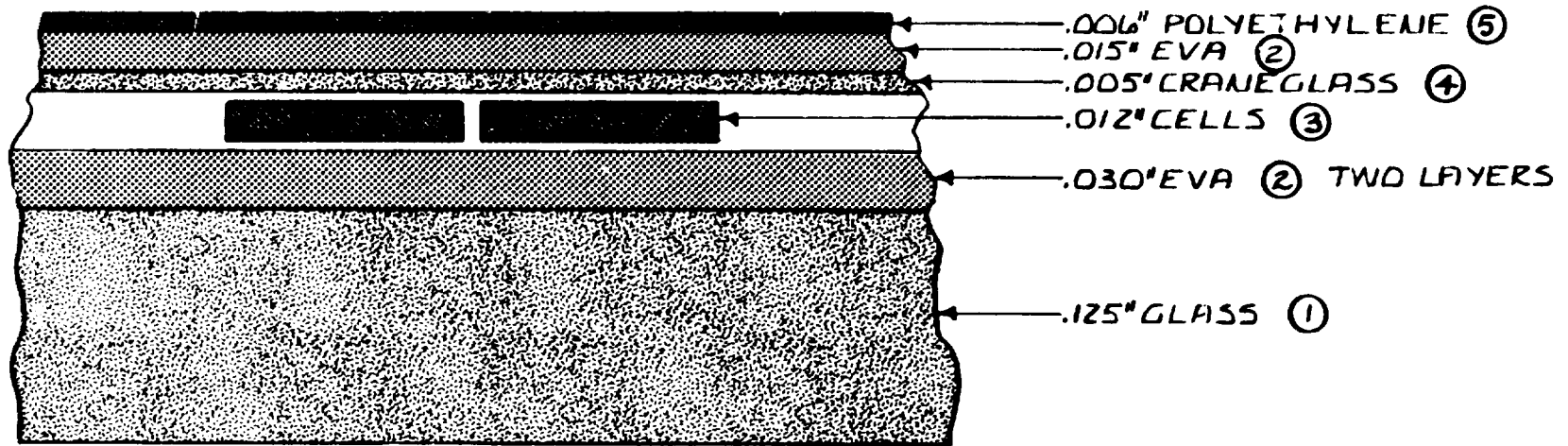


Figure 9

Module Cross-Section

SIDE VIEW



NOTE:  
TOTAL THICKNESS BEFORE  
LAMINATION .193"

SECTION A-A

- Is compatible with the process and the other materials in the module.

We have considered a variety of glasses, including tempered and annealed, 1/8 in. and 3/16 in. thick and a variety of iron contents: Sunadex (0.01% Fe), Solatex (0.05% Fe) and soda lime (0.2% Fe). While 1/8 in. annealed soda lime is the most economic for the MEPSDU program, questions about its structural ability remain to be answered.

Ethylene vinyl acetate (EVA) has been chosen as the encapsulant. Its main advantages are its low cost and ease of use in the lamination process. EVA does have the following required properties:

- It does not degrade under UV exposure when protected by glass.
- It can withstand the necessary thermal cycling conditions.
- It can mechanically protect the solar cells.
- It and its processing are compatible with the other materials in the module.

We will use two sheets of 0.018 in. thick EVA between the glass and the cells and one sheet of 0.018 in. thick EVA behind the cells.

Craneglass has been included in the module because it:

- Aids in the removal of bubbles during lamination,
- Improves the electrical insulation of the module,
- Lessens cell movement during lamination,
- Results in a smoother module back.

The very low cost of the Craneglass makes its use feasible wherever needed.

Linear low density polyethylene film is recommended as the vapor barrier because it:

- Has a low value of permeability to water vapor,
- Is tough and puncture resistant,
- Has demonstrated a long lifetime in outdoor applications (up to 30 years),
- Has sufficient dielectric strength to meet all codes,
- Is compatible with the processes and other materials,
- Has a very low cost.

A 0.006 in. thick black polyethylene film made with minimum memory will be utilized.

The electrical output of the module will be accomplished by use of a Solarlok connector designed specifically for



photovoltaic modules. Figure 10 shows the design of these connectors. The ease of installation, the ease of module interconnection in the field, and the low cost make this connector ideal for the MEPSDU module.

Rather than providing the module with a frame, we will seal and protect the edge of the module with a gasket. The gasket can save the cost of the integral frame and can be attached in the field as cost effectively as a hard frame.

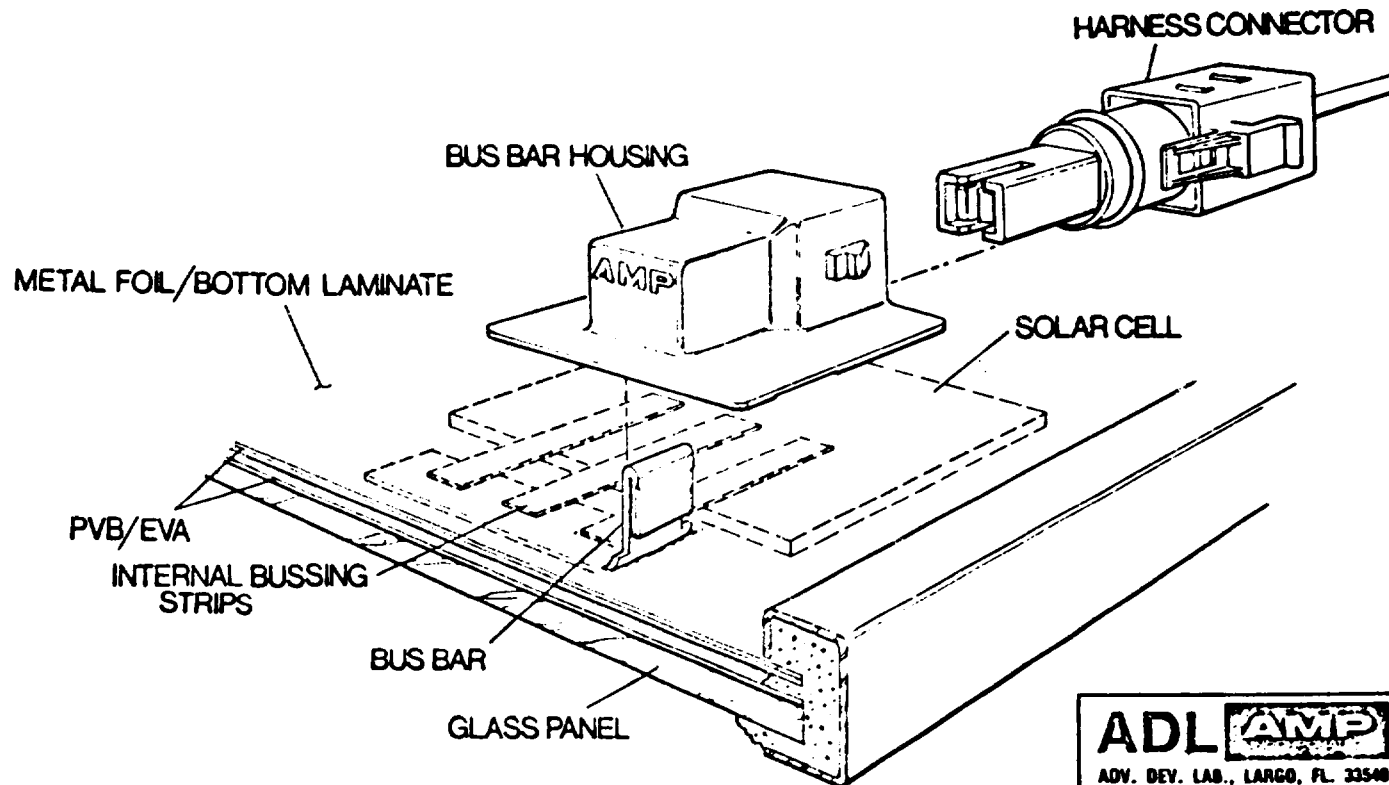
The preliminary cost estimate for the materials in the module is \$0.0488/Watt for the encapsulation materials and \$0.025/Watt for the AMP connector system.

Utilizing 36 series strings of two parallel 10 cm. x 10 cm. semicrystalline solar cells results in a module design voltage of 14.5 volts at peak power and NOCT. This is ideal for use in battery charging systems (12 volt) or for use in higher voltage systems.

The initial module design called for standard over-under interconnection with only two pads per cell, both on one edge. This design has no crack tolerance, may have insufficient stress relief in the high density package, and results in lower cell efficiency because of the large travel distance required of carriers across the cell face. To improve the design, we have elected to use a wraparound type of contact with four pads on every cell. Then there are four front and

Figure 10

SOLARLOK CONNECTOR SYSTEM



PRELIMINARY

5/1/80

four back contacts, providing good crack tolerance. Putting two pads on two opposite edges means that each 10 cm. x 10 cm. cell acts like four 5 cm. x 5 cm. cells, resulting in higher efficiency. Having both wraparound and in plane stress relief improves the stress relief properties of the module. The design of the interconnects are shown in Figure 11. This one piece wraparound interconnect minimizes equipment complexity and cost with material cost being well within the cost requirements.

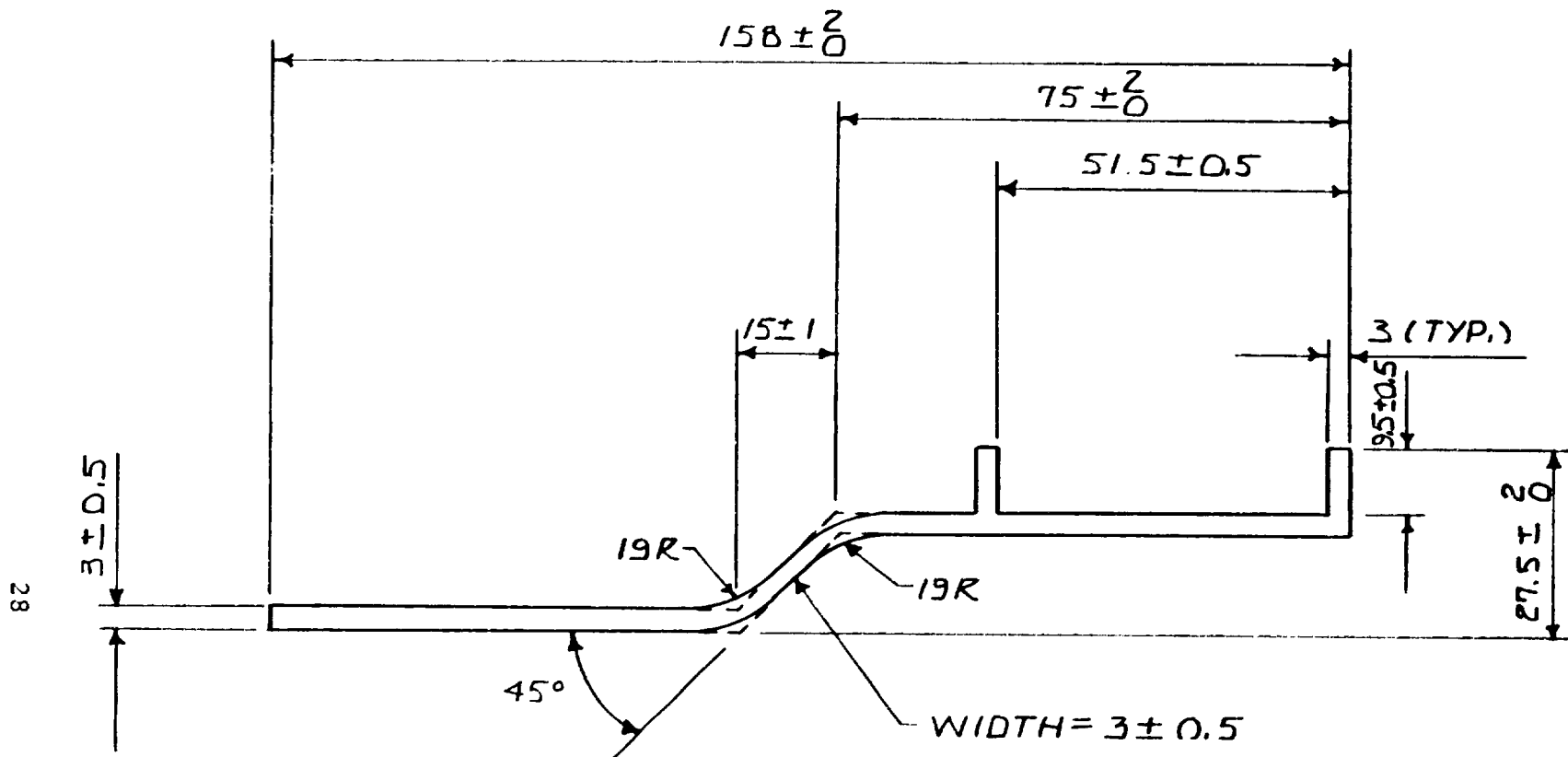


Figure 11. MEPSDU Interconnect

## 2.4 Tapping and Stringing Machine Design

Kulicke and Soffa Industries, Inc. is to design, build and deliver the automated tapping and stringing machine required to assemble the 10 cm. square solar cells into series connected strings, and place the strings in a module array format. The machine should accommodate the module layout described in the previous section. The target machine cycle time is five seconds per cell with a yield of 95% or better. The bonding technique to be used is pulsed heat solder reflow.

Figure 12 shows a flow diagram for the proposed machine. In the proposed machine to be built (Figure 13), cells would be automatically dispensed from cassettes and aligned prior to entering the machine. A walking beam conveyor system, which maintains cell registration, transports the cells through the various initial process stations.

The cells would first enter an insulating station that applies strips of adhesive backed tape to the back of each cell.

Next, a fluxing station applies flux to bond sites on the top side of each cell using a stamp pad technique or metered dispensing system. The cells would then enter the interconnect stations, where the one-piece stamping interconnects are fed, sheared, and transferred into position over the cells, then solder bonded to each cell using a pulsed heat bonding technique.

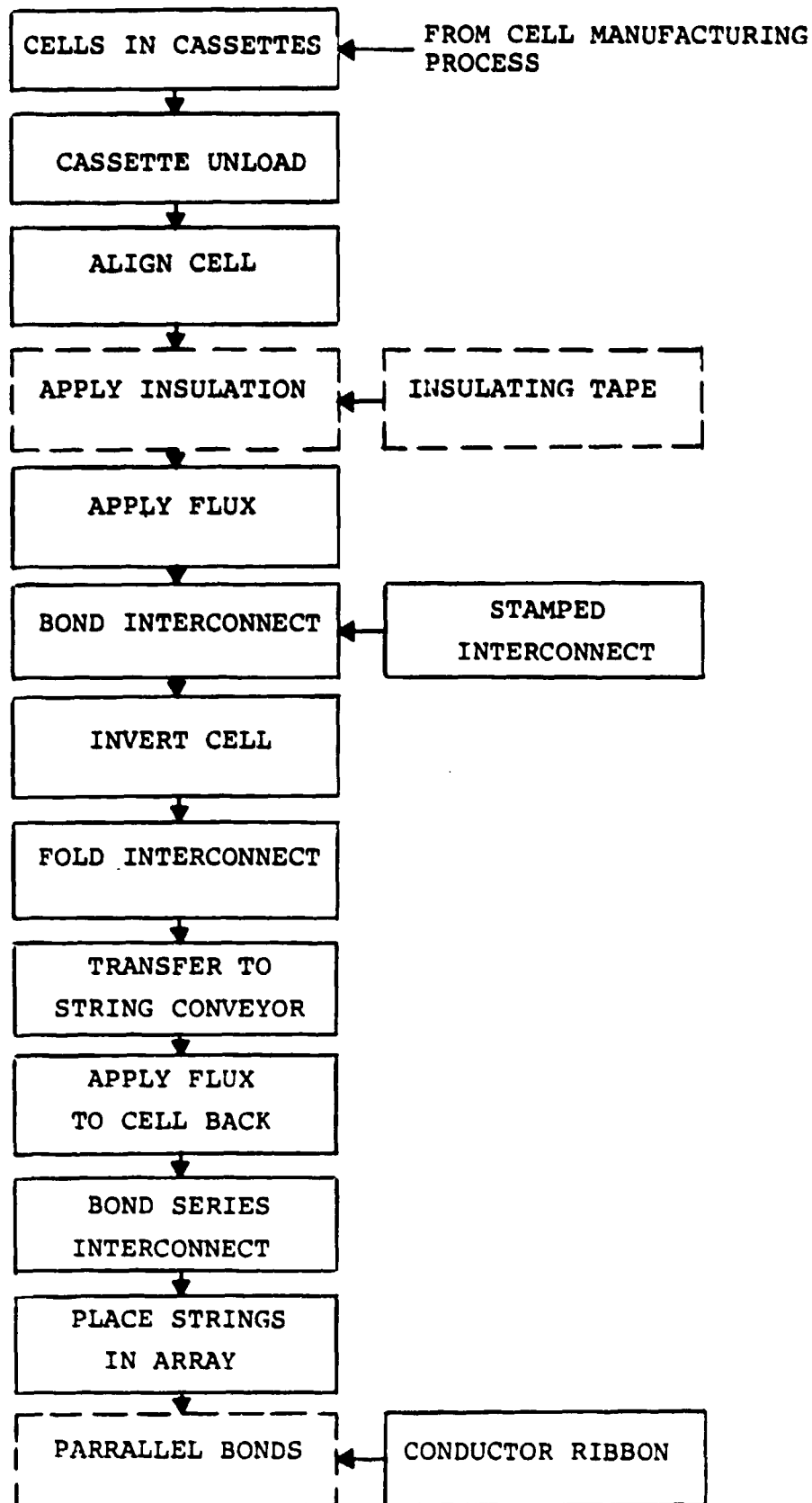


Figure 12. Flow Diagram of Tapping and Stringing Machine

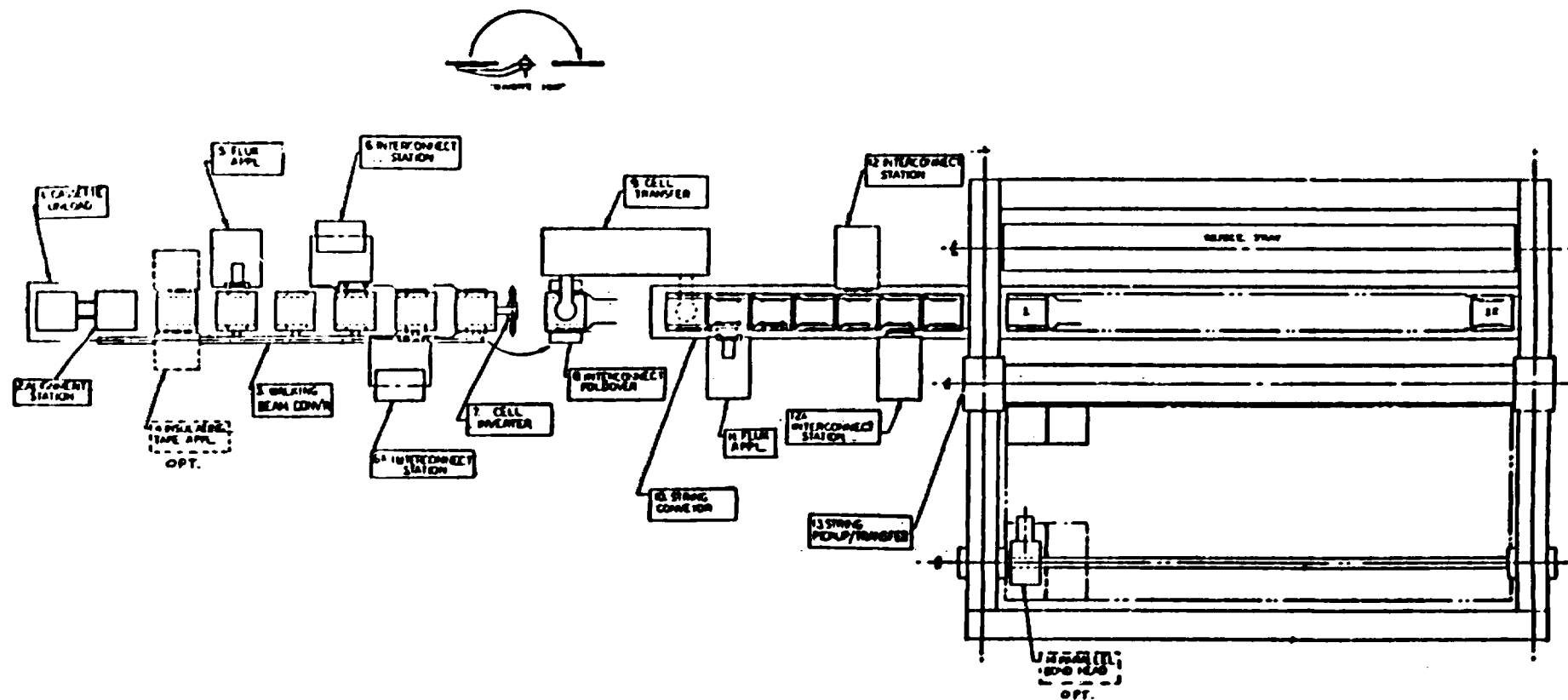


Figure 13. K&S Automated Tabbings and Stringing Machine

After interconnects are bonded to the cell face, the conveyor moves each cell to an inverter station, which turns the cells over (upside down) prior to the stringing operations. An interconnect foldover station then positions each cell and folds the interconnect over to the cell back for series bonding operations. The cells are then transferred onto a string conveyor, which maintains inter-cell registration while indexing the cells through the stringing operation to the discharge area of the machine.

The cells would then enter a second fluxing station, which applies flux to the cell back, and proceed to the second interconnect stations, where the cells are joined together into strings. A string pickup and transfer station would automatically pick up completed strings and place them in the module array area. This station has a track mounted vacuum lance which can rotate to accomodate string reversal. A reject tray is provided in the discharge area in case it is determined that the cell string should not be delivered to the module array area.

While in the module array area, parallel connections between strings and buss bar attachments can be made with a traversing bond head. These are optional and still under discussion with Solarex as to the most cost effective way of accomplishing these tasks.



A more detailed description of the various machine stations follows.

#### 2.4.1 Station 1: Cassette Unload Station (Figure 14)

The cassette unload station will accomodate up to four cassettes, containing 25 cells each, stacked vertically. The cassettes are to be able to be loaded while the machine is operating, and empty cassettes will be automatically ejected to a collection area where they may be removed for reuse.

#### 2.4.2 Station 2: Cell Alignment Station (Figure 14)

In this station, the cell will be aligned to achieve proper registration before being indexed through the machine for functional operations. Each cell is moved into the cell alignment station from the cassette unload station. A mechanism will push the cell into proper registration against the aligning pins.

#### 2.4.3 Station 3: Walking Beam Conveyor Station (Figure 15)

This station indexes cells accurately from station to station using a "handshake" technique. Vacuum cups contact the cell backs gently, and a central pickup approach allows access to cell edges for functional purposes.

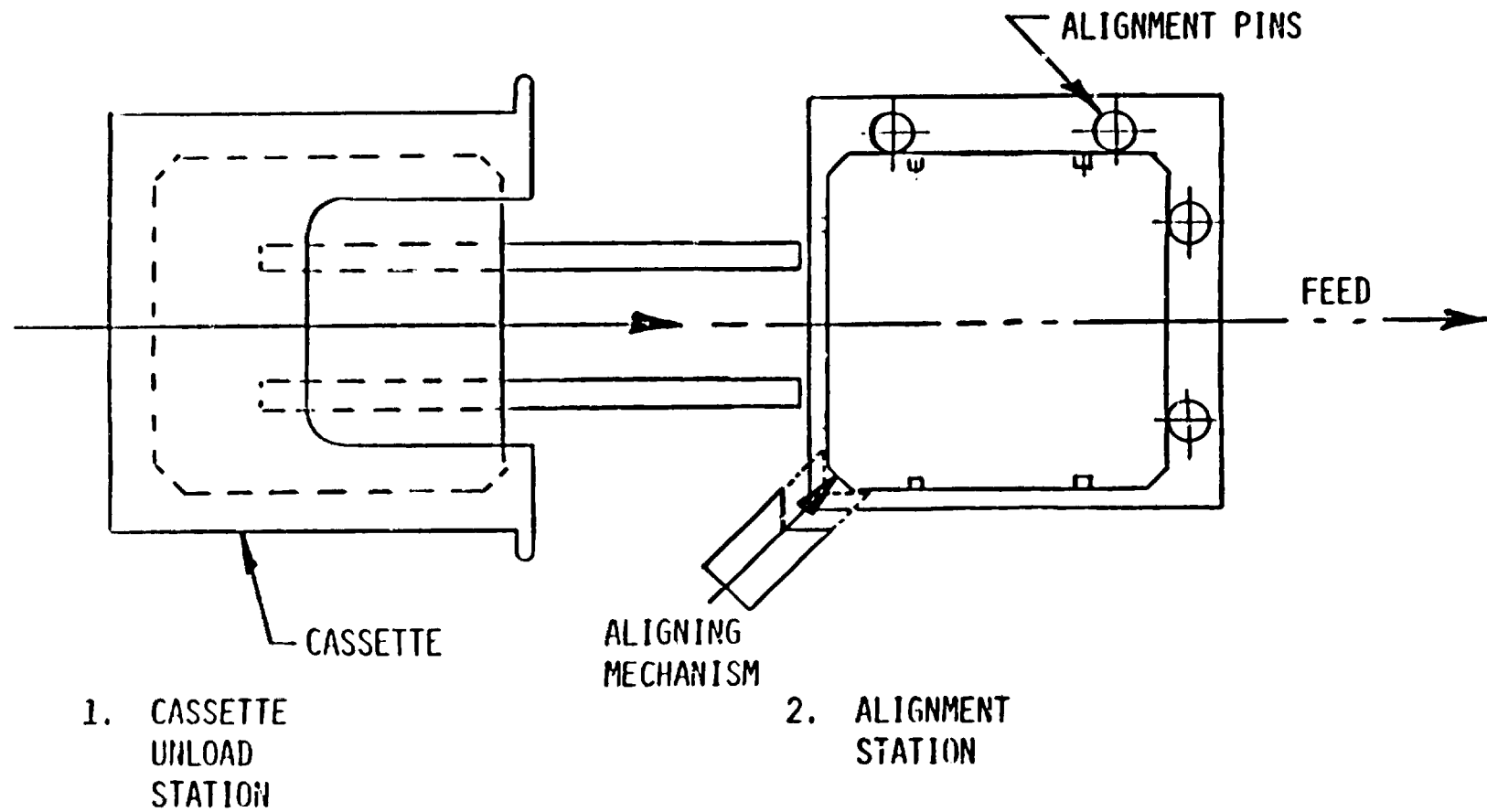


Figure 14. Unload and Alignment Stations

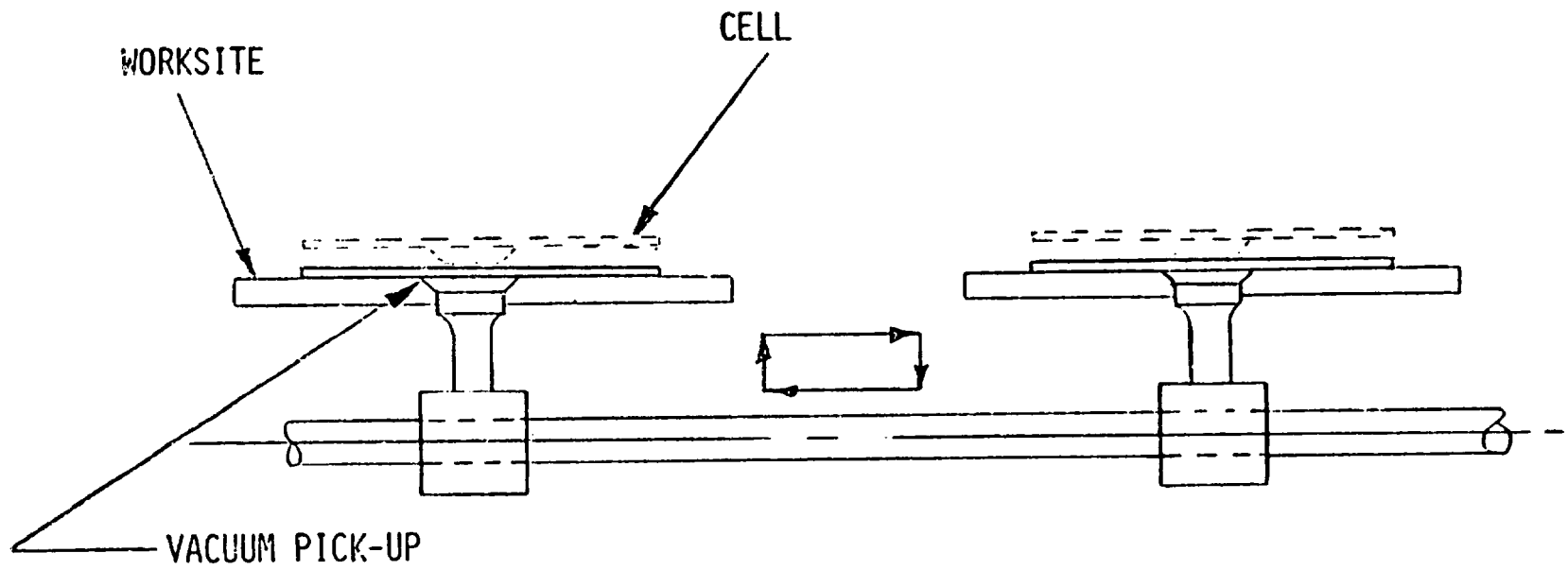


Figure 15. Walking Beam Conveyor

#### 2.4.4 Station 4: Insulating Tape Application Station

(Figure 16)

As now envisioned, this insulating station feeds pre-cut adhesive backed tape to an applicator head. Two heads are to be used; one for each side of the cell back. The exact material and configuration of the insulating tape is under study.

#### 2.4.5 Station 5: First Flux Application Station (Figure 17)

This station would apply a proper amount of flux to the bond sites on the collector side of each cell, using a stamp pad technique, or alternatively, a metered dispensing system.

#### 2.4.6 Station 6 and 6A: First Interconnect Stations

(Figure 18)

In these stations, die stamped, pre-tinned copper interconnects are carried on a roll between the layers of protective paper. The interconnect stations (one for each side of the cell) cut and feed the interconnects from the roll, position the interconnects over the bond sites, and solder bond them to the cell.

#### 2.4.7 Station 7: Cell Inverter Station (Figure 19)

This station inverts the cell prior to the stringing operations. The inverter pickup arm holds the cell by vacuum

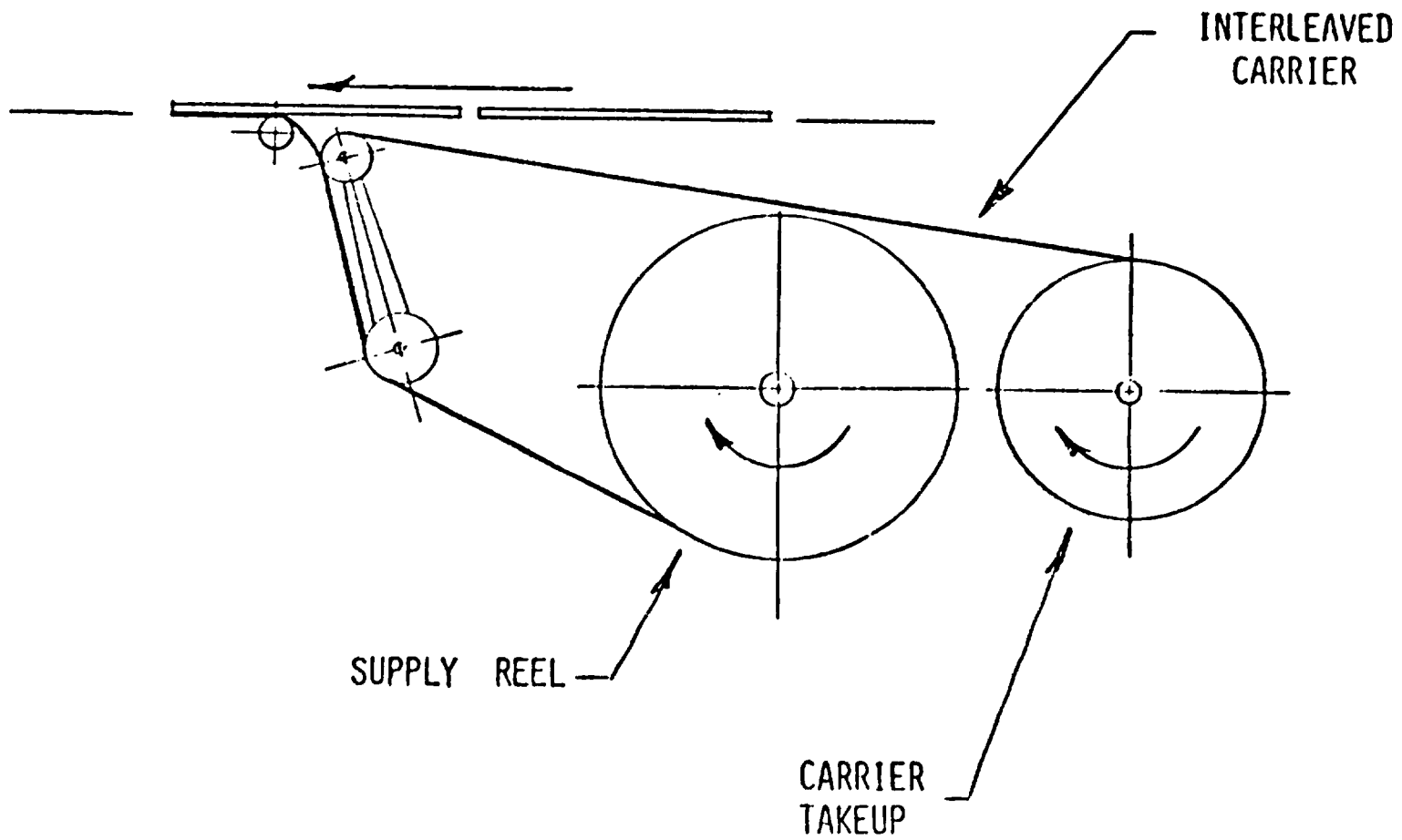


Figure 16. Insulating Tape Application Station

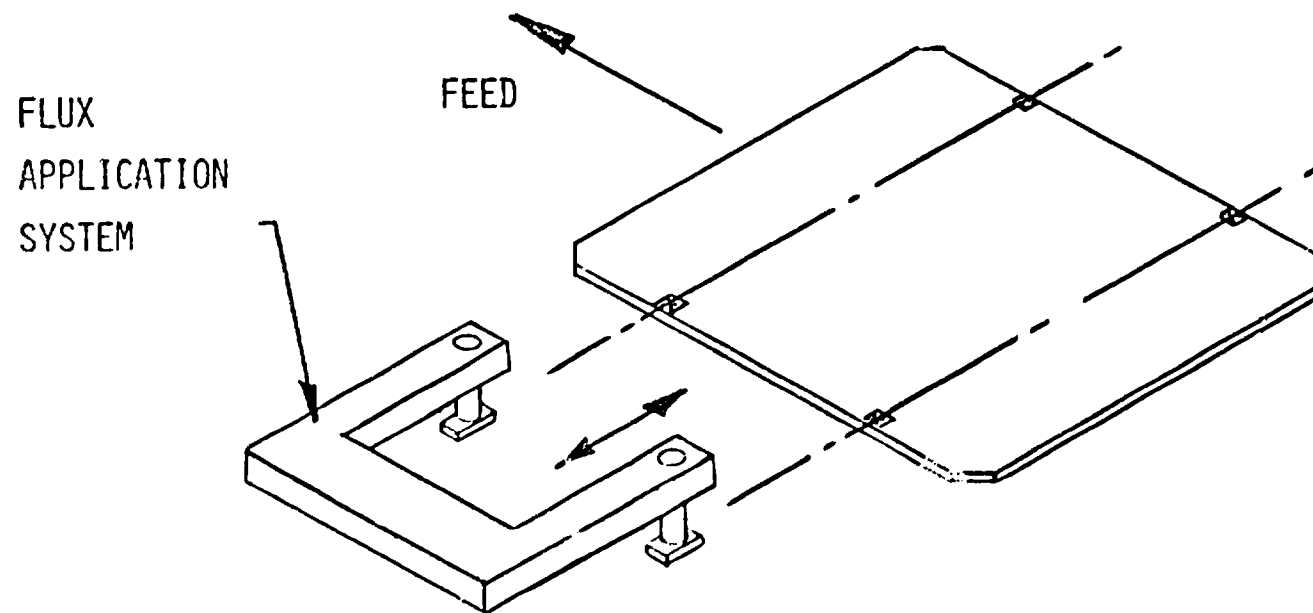


Figure 17. First Flux Application Station

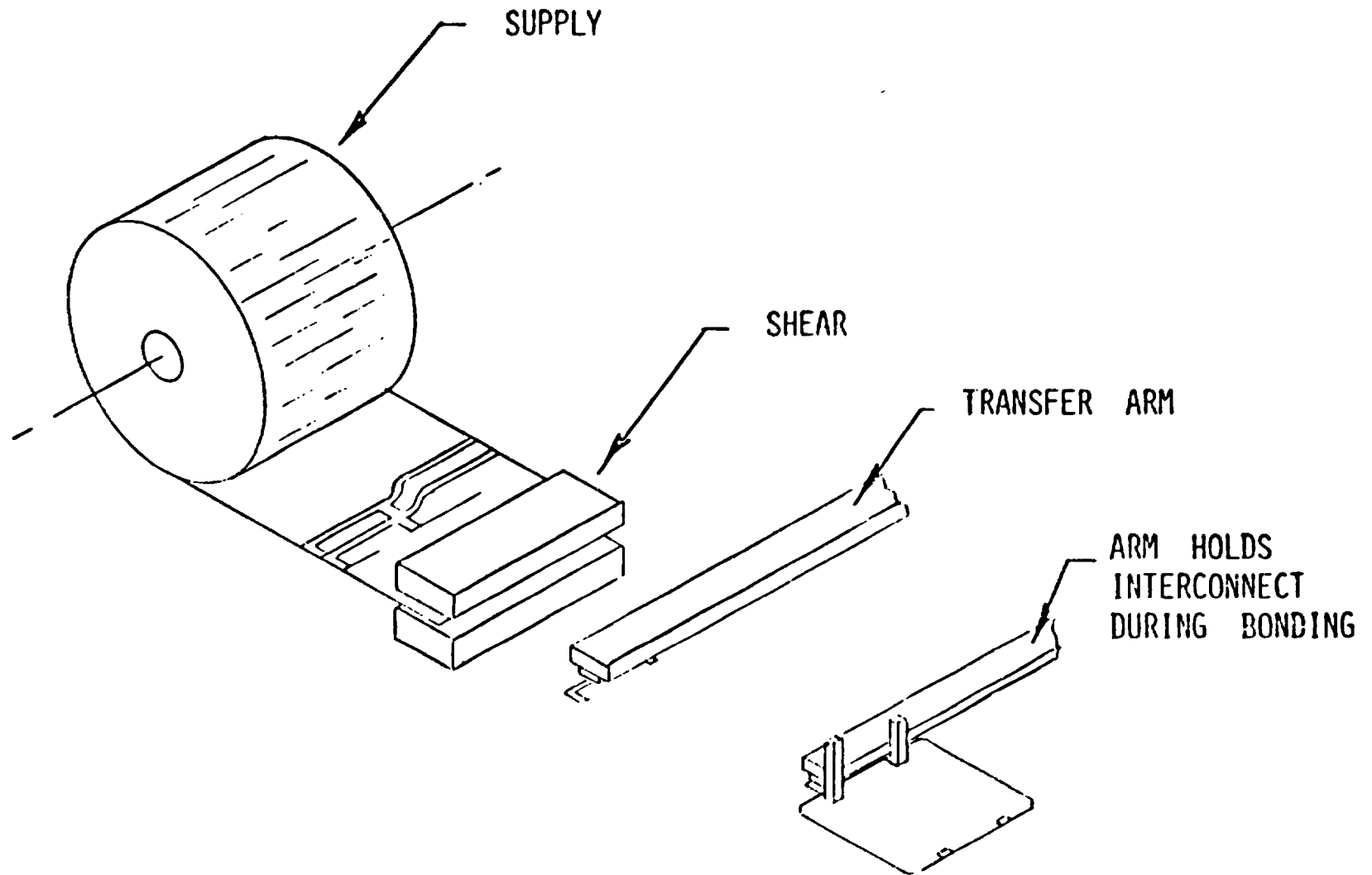


Figure 18. First Interconnect Stations

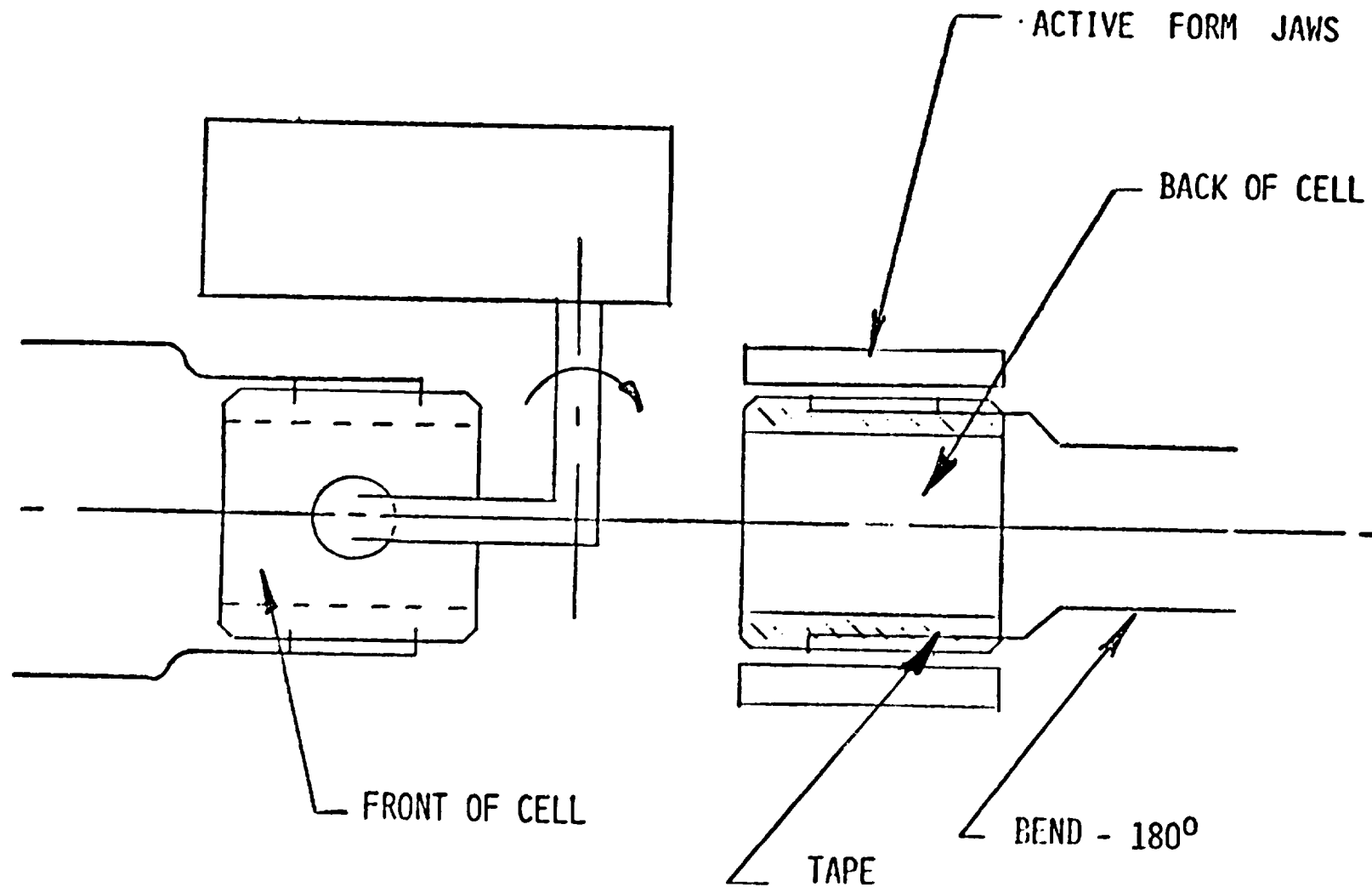


Figure 19. Cell Inverter Stations



on its back until it accomplishes the inverting action. After depositing the cell on the holding stage of the interconnect foldover station, the inverter arm will return to receive the next cell.

#### 2.4.8 Station 8: Interconnect Foldover Station (Figure 20)

This station contains two forming jaws which fold a portion of the stamped interconnect over onto the cell back in readiness for making the stringing connections.

#### 2.4.9 Station 9: Cell Transfer Station (Figure 21)

To move cells from the foldover station to the string conveyor, the transfer station will use a vacuum arm to lift the cell and place it on the first position of the string conveyor to be joined with other cells in a string.

#### 2.4.10 Station 10: String Conveyor (Figure 22)

The string conveyor will consist of a stainless steel conveyor belt centrally located under the cell travel path. Locating fixtures, mounted on the belt, engage the cells on their edges only. The string conveyor holds the location of the cells and maintains their registration between each other within each string. The conveyor will be programmed to advance the cells one inter-cell pitch after the second interconnects are made. Upon completion of each string there will be a double index to create a separation between strings for further handling, as in the string pickup system.

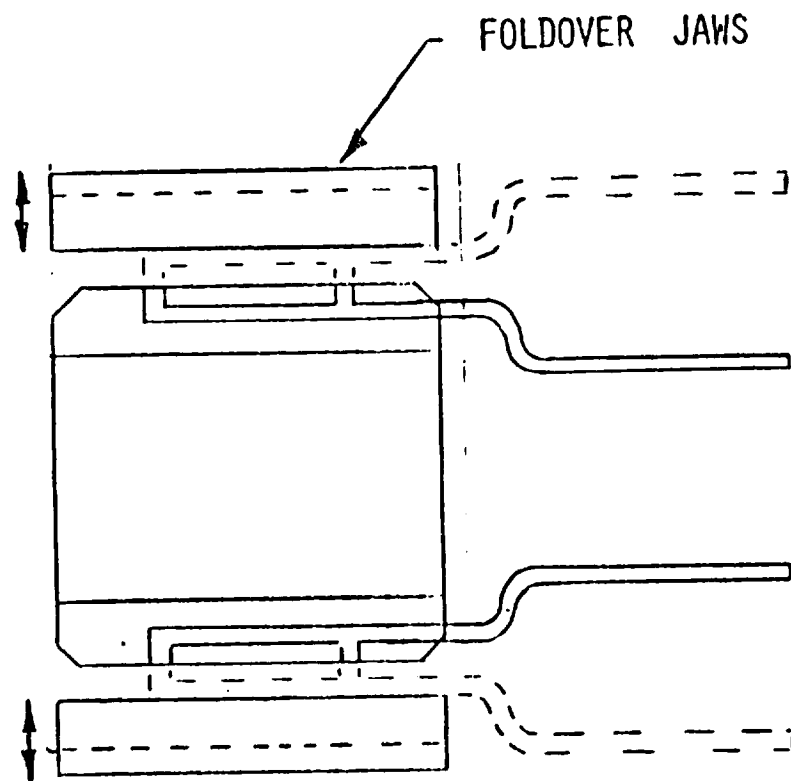


Figure 20. Interconnect Foldover Station

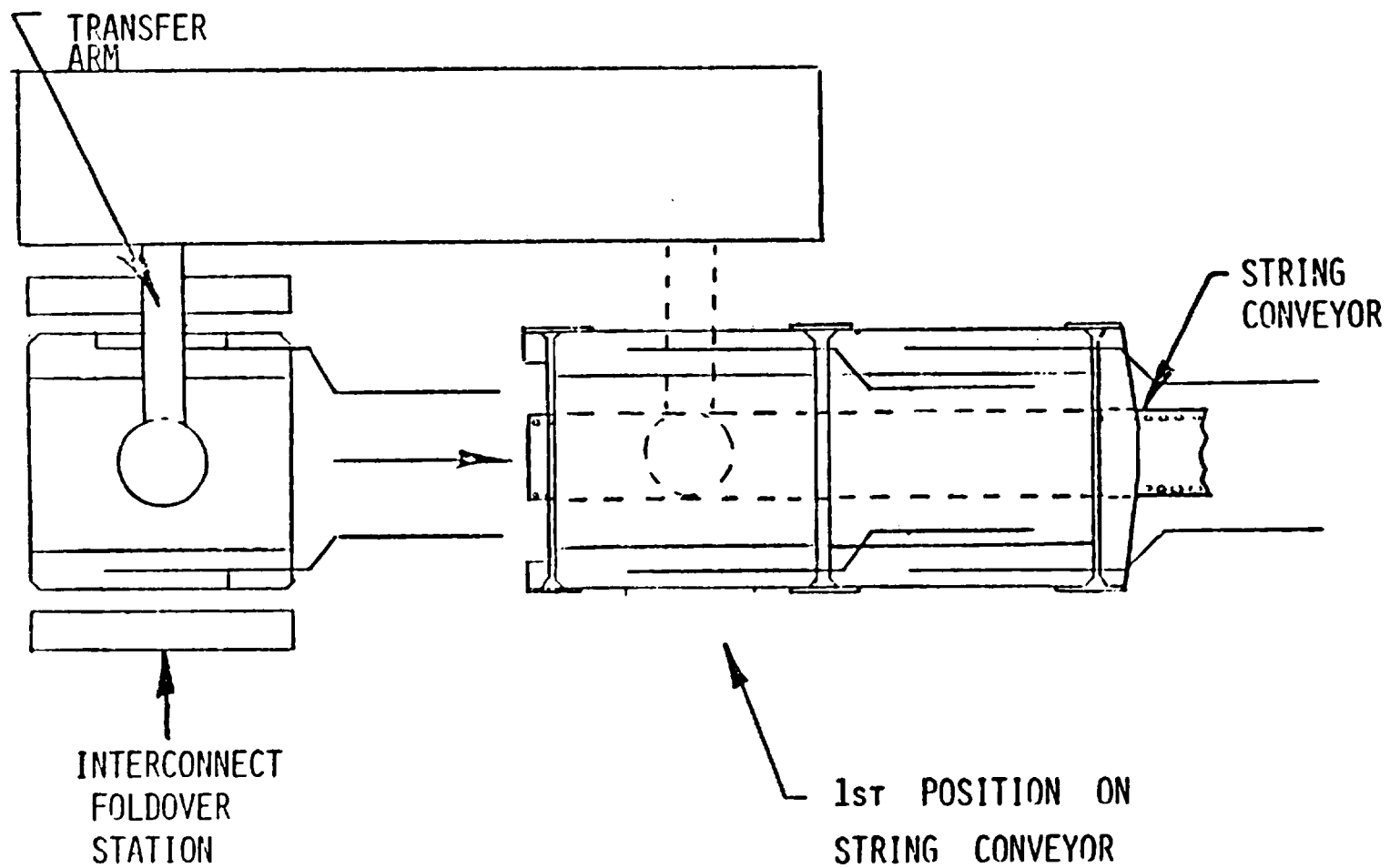
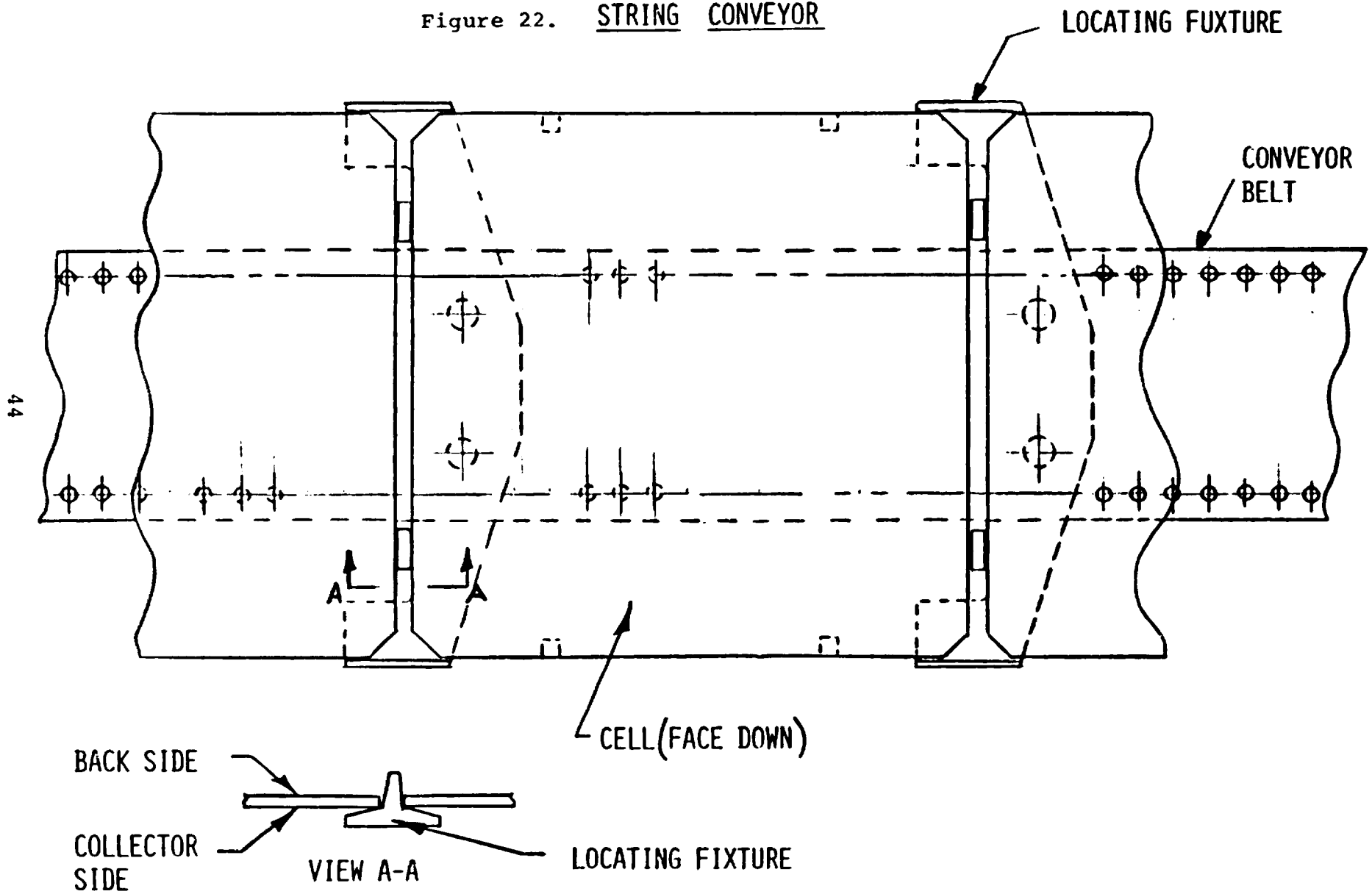


Figure 21. Cell Transfer Station

Figure 22. STRING CONVEYOR



**2.4.11 Station 11: Second Flux Application Station**  
(Figure 23)

The second flux application station in the system applied flux to the back side of the cell by means of a stamp pad or metered dispensing mechanism, in the same manner as Station 5 (Section 2.4.5).

**2.4.12 Station 12 and 12A: Second (Stringing) Interconnect Station (Figure 24)**

Connecting cells in series (stringing) will be accomplished by this station using two pulsed heat reflow soldering systems for each side of the cell. These systems bond extending portions of the folded interconnect to the adjacent cell.

**2.4.13 Station 13: String Pickup and Transfer Station**  
(Figure 25)

This station uses a track mounted, multi-headed vacuum lance to automatically pick up completed strings after they have been indexed into this area by the string conveyor. The vacuum lance will maintain the proper inter-cell mechanical spacing of the strings and the track will be provided with detents to maintain correct inter-spring spacing in the module area. The vacuum lance will be able to be rotated to accomplish reversal of strings prior to their being placed in the

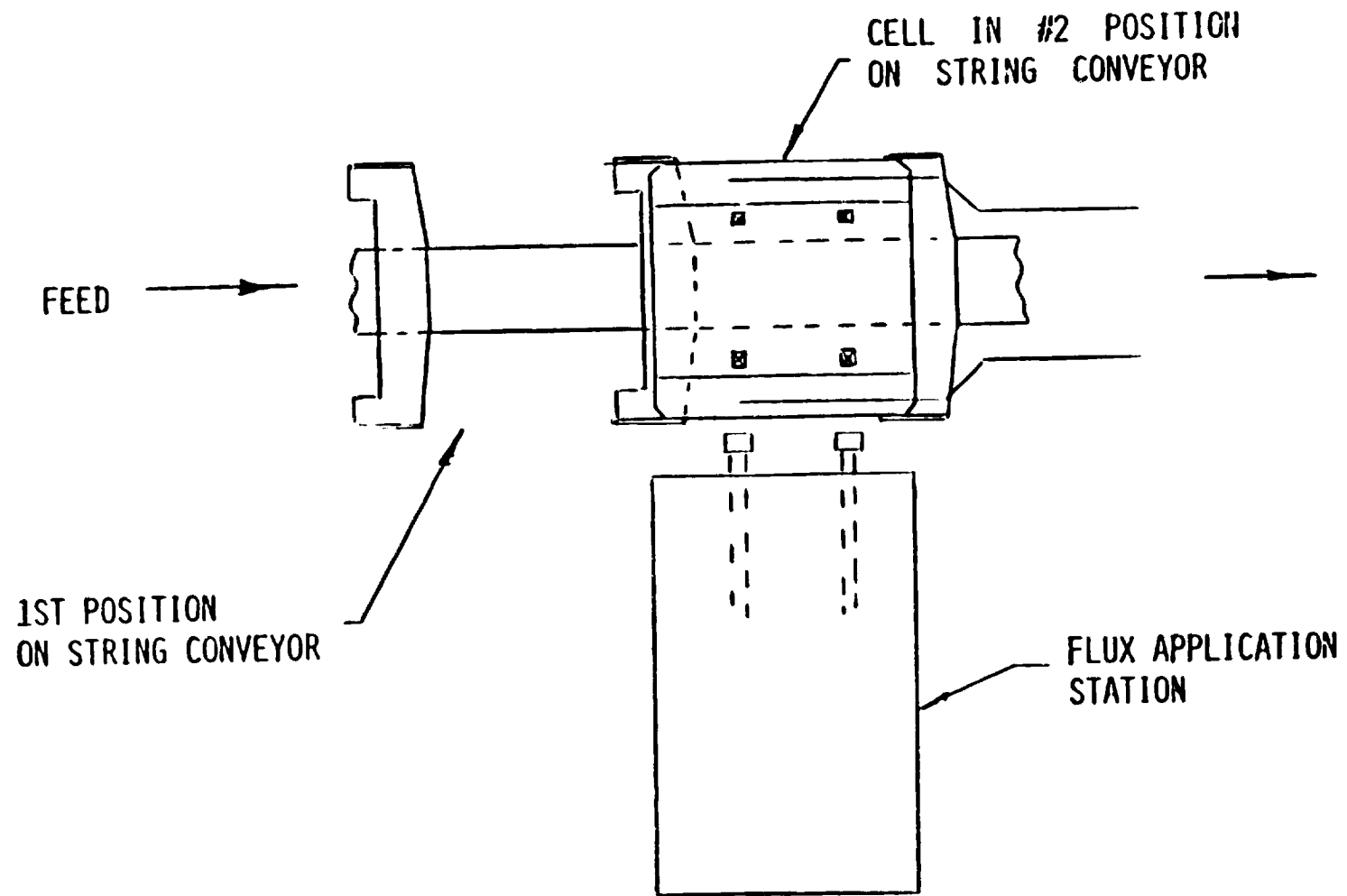


Figure 23. Second Flux Application Station

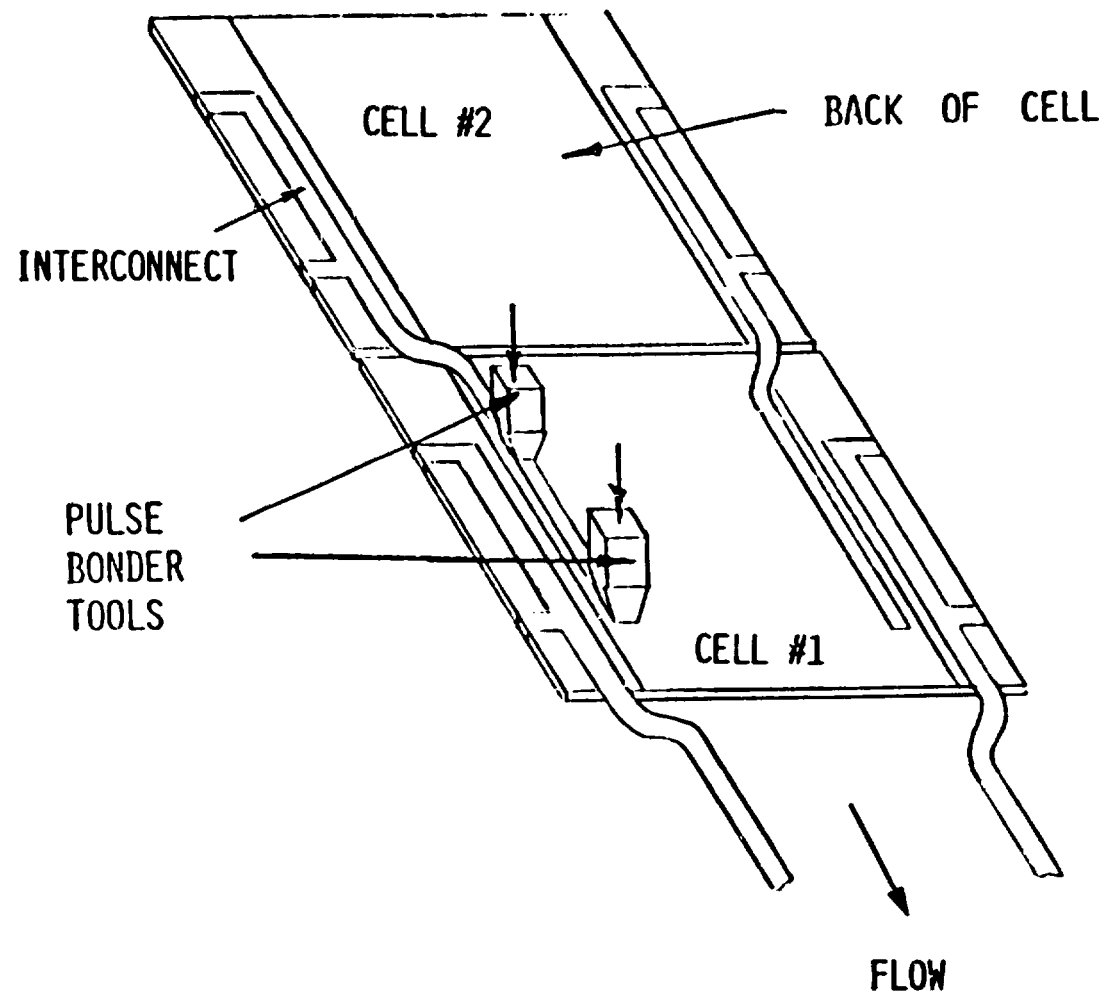


Figure 24. Second (Stringing) Interconnect Stations

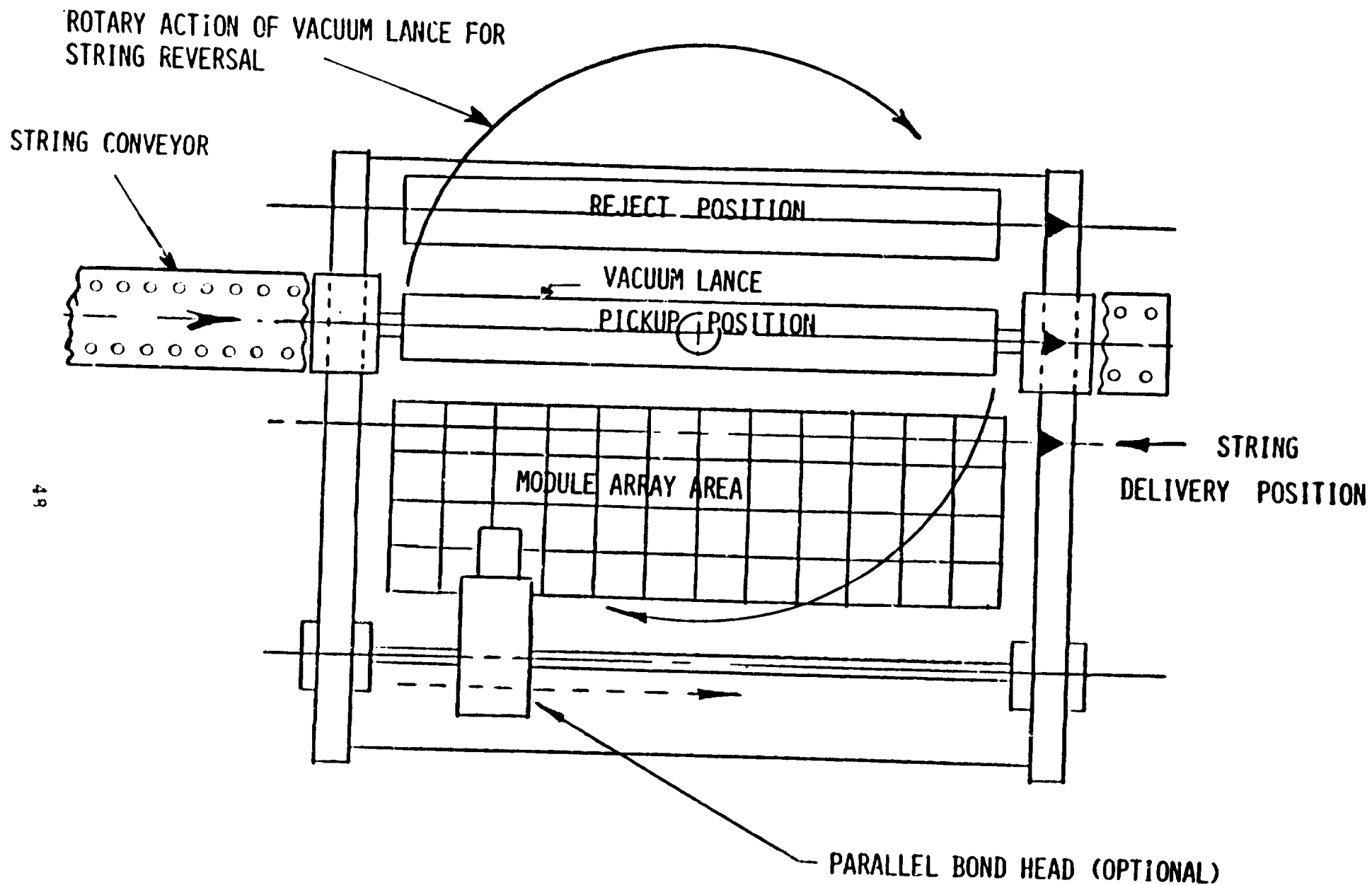


Figure 25. STRING PICKUP AND TRANSFER STATION



module array area. A reject tray will be provided in the discharge area in case it is determined that the cell string should not be delivered to the module array area. The final arrangement of this station is to facilitate integration with the rest of Solarex's overall module manufacturing process.

#### 2.4.14 Station 14: Parallel Bond Head - Optional (Figure 17)

A traversing parallel bond head may be incorporated in the module array area to accomplish the parallel connections between strings. The specific manner and location of accomplishing this task is still being studied to determine the most cost effective method in conjunction with the number of parallel connections to be made.

#### 2.4.15 Machine Control System

The control circuitry intended to be utilized for the machine is a programmable controller that is compatible with, and can be enhanced by, microprocessor and servo circuitry.

## 2.5 Module Encapsulation

The process flow sequence for module encapsulation is shown in Figure 26. The cell string will be transported on a belt through a rinse system where water flux neutralizer and water again will be sprayed. The glass will also be transported on a belt. It will be steam cleaned, dried and primed. The module will be layed up manually using roll out dispensers for the various layers.

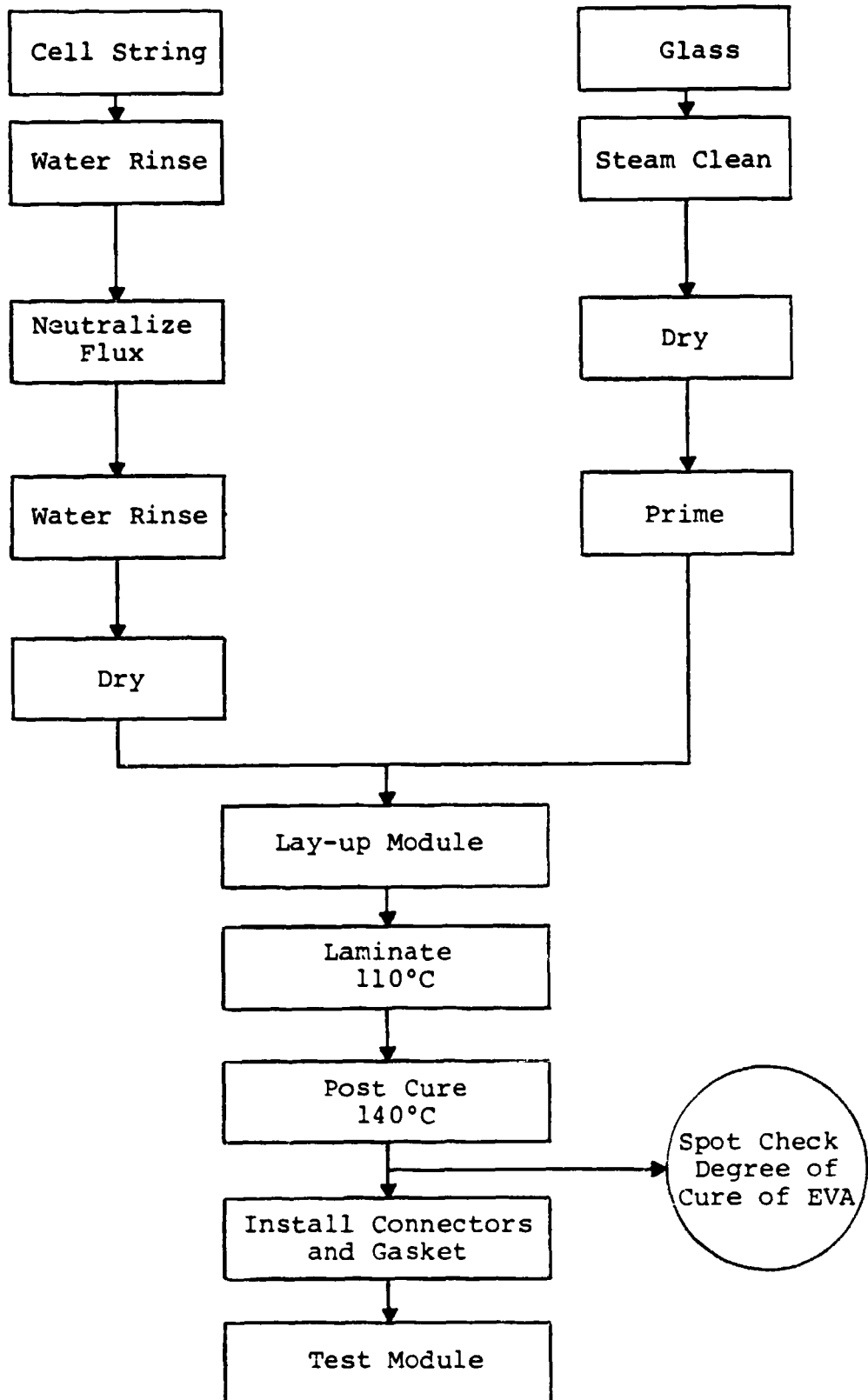
The module will be laminated in an evacuated chamber for a minimum time, just enough to remove the air from between the layers and have the EVA molten long enough to make good contact with all of the components. The EVA will then be cured in an oven where many modules can be cured at the same time.

The AMP connectors and the gasket will then be attached manually.

This lamination procedure has been adopted over other techniques because:

- With large modules and cells, breakage is a problem unless the laminating force is exerted evenly and slowly.
- The long cure time required for EVA would mean excessive time in expensive laminators.

Figure 26. MODULE ENCAPSULATION



- Temperatures higher than 140°C result in bubbles in the EVA.

The preliminary cost estimate yielded a lamination cost of \$0.1356/Watt, which includes the materials costs listed in Section 2.3.

## 2.6 Test System

Every solar cell and every module will be tested under illuminated conditions to draw an IV curve to provide a measure of power at the design voltage and to provide all the data for statistical analysis. The individual systems are described below.

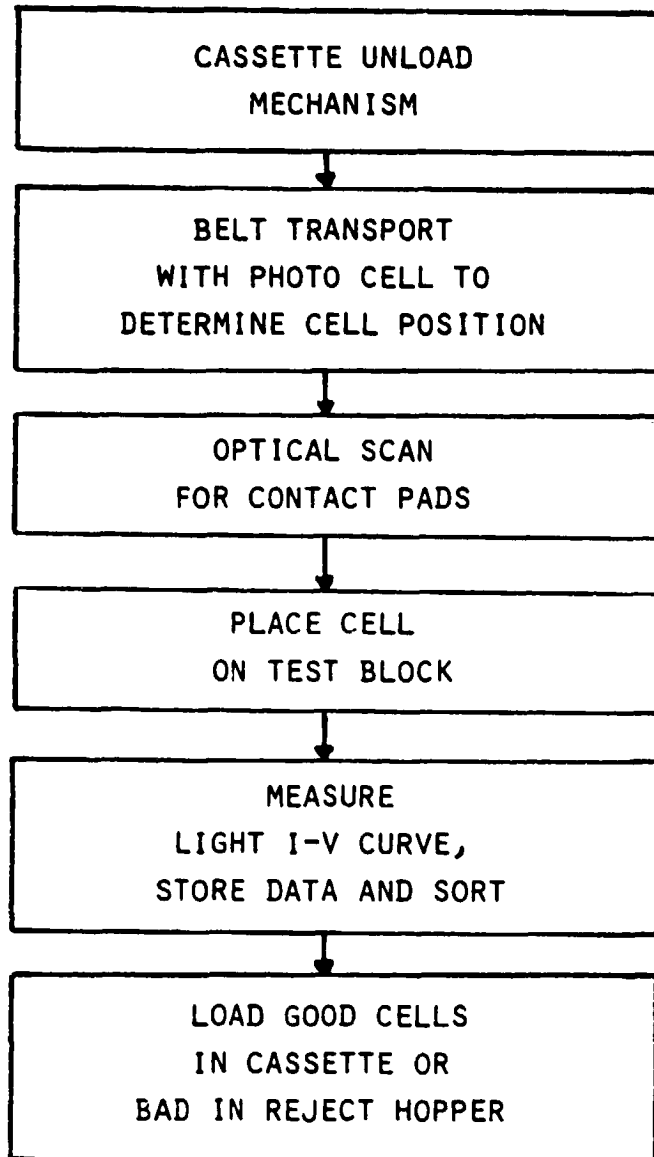
### 2.6.1 Cell Test System

The process sequence of the cell test system is shown in Figure 27. The cells are unloaded from a cassette, transported on a belt, optically scanned to assure that the contact pads are in place, placed on a temperature controlled test block, illuminated by a Xenon source, a light IV curve taken, and the good cells loaded back into cassettes. A block diagram of the test system is presented in Figure 28. The Cell Test Subsystem Components and the Data Flow are shown in Figure 29. The components are recommended based upon their use in similar test systems now in operation. The computer controlled testing will follow the flowchart overview shown in Figure 30.

### 2.6.2 Module Test System

The process sequence of the module test system is shown in Figure 31. The modules are manually loaded onto a light table and connected electrically to the system. The operator then initiates the computer, which draws the IV curve, stores

Figure 27  
CELL TEST PROCESS SEQUENCE



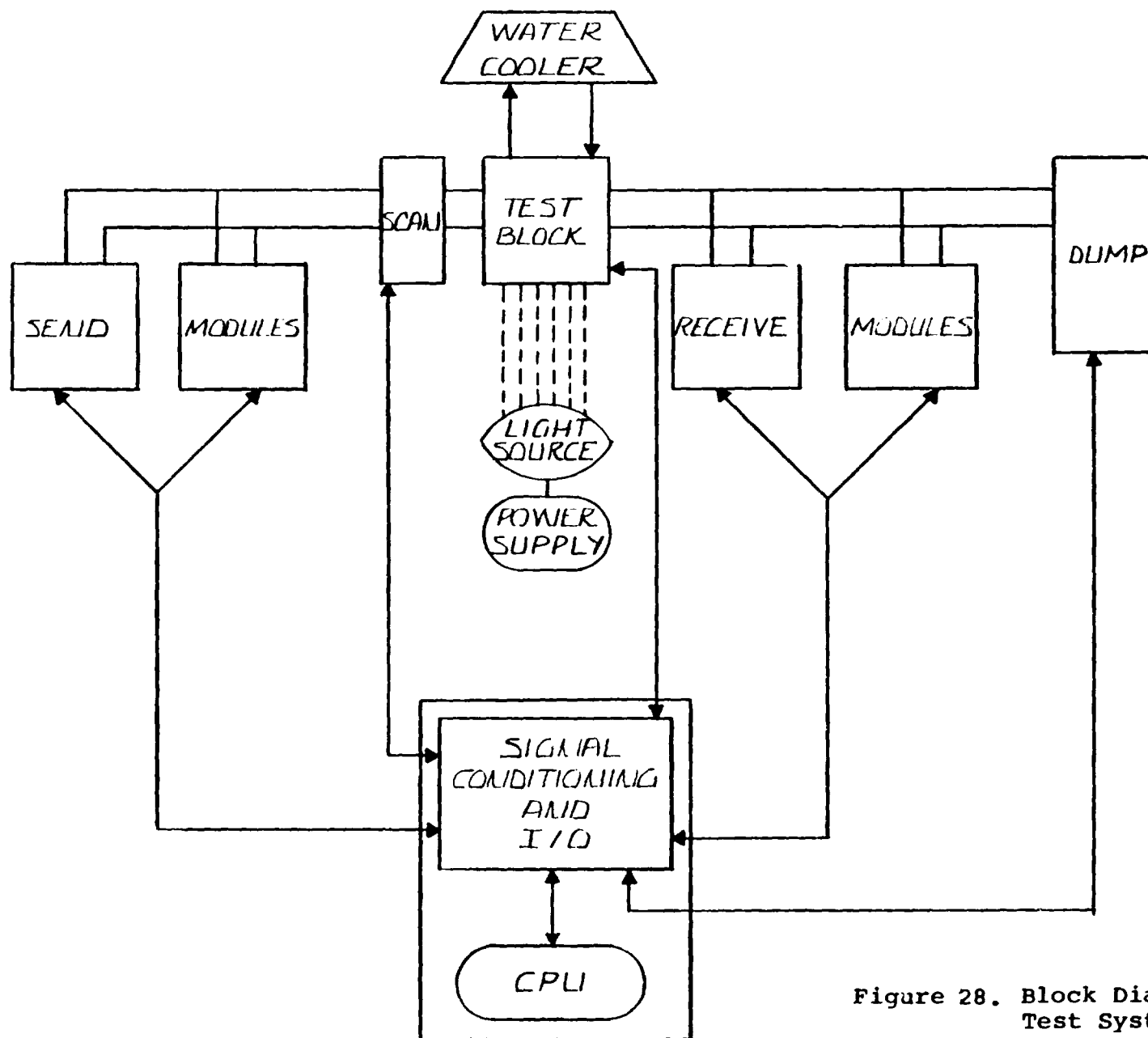


Figure 28. Block Diagram of Test System

# CELL TEST SUBSYSTEM COMPONENTS AND DATA FLOW

56

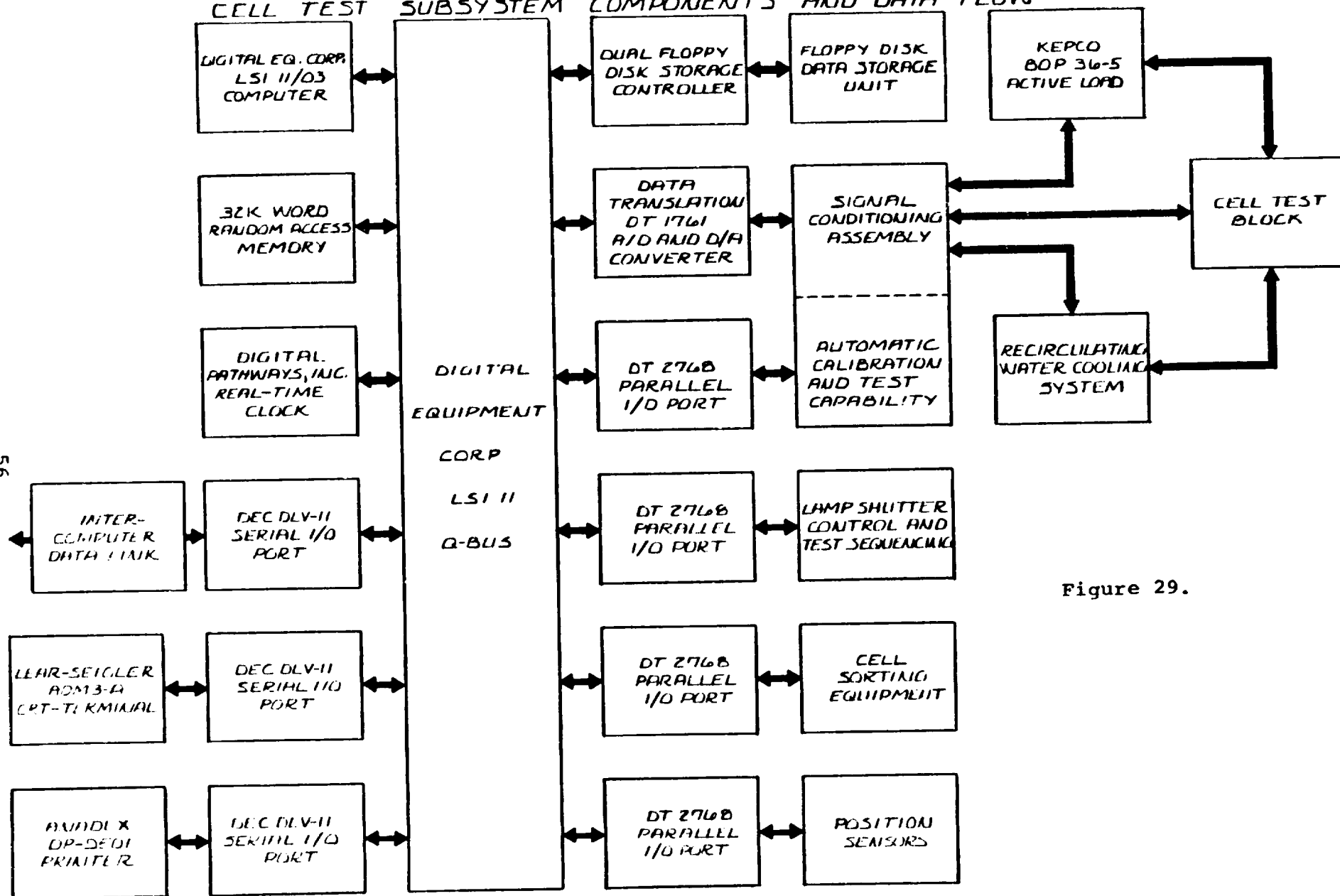


Figure 29.



Figure 30. CELL MEASUREMENT OVERVIEW  
FLOWCHART

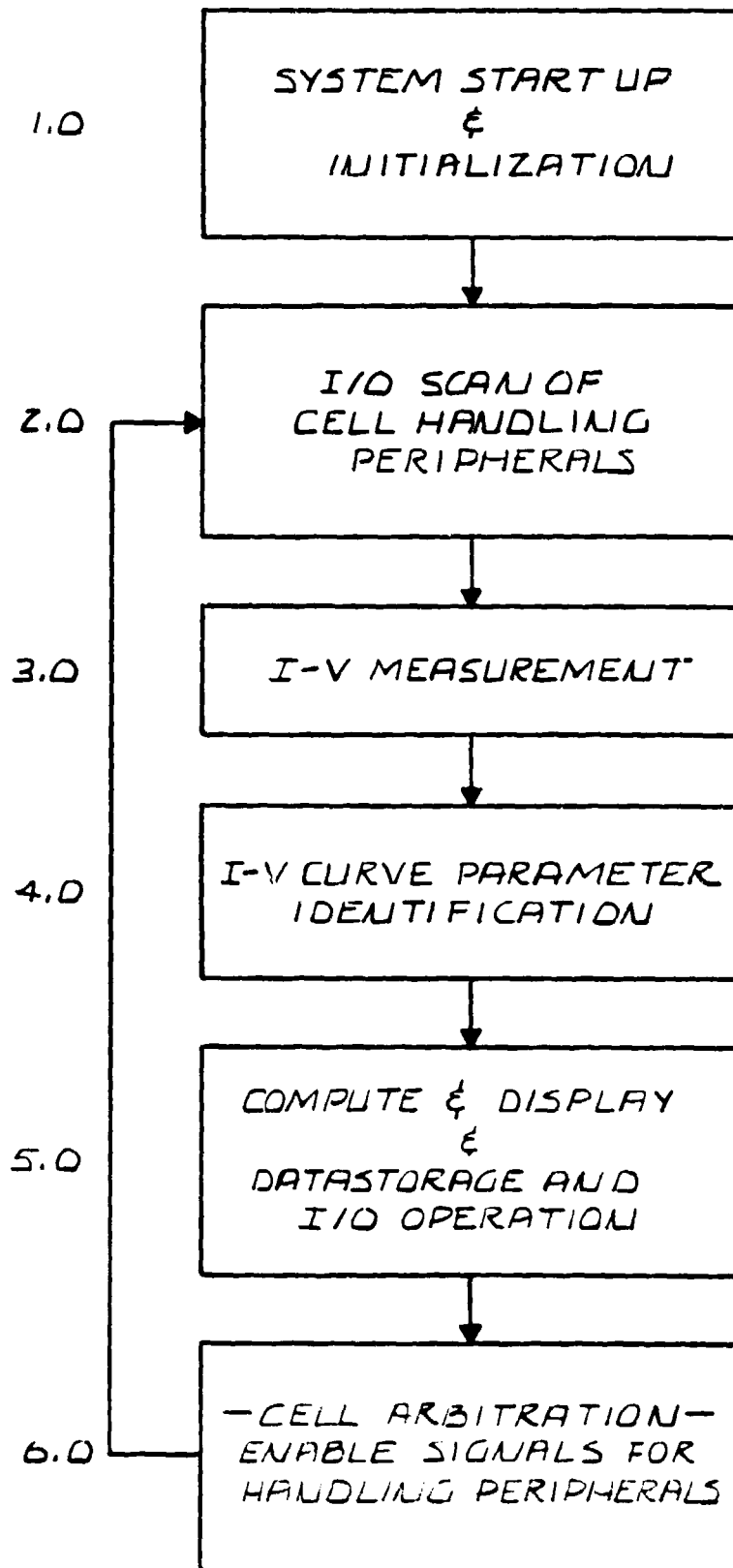
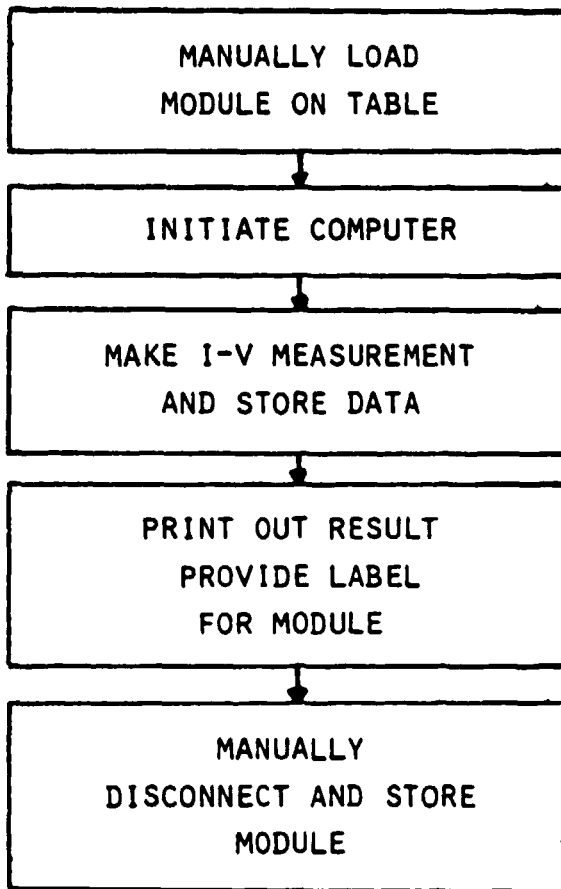


Figure 31.

## MODULE TEST SYSTEM

### PROCESS SEQUENCE



the data, and prints out a label for the module, including the model number, serial number and power measured at the design voltage. The operator then disconnects the module, applies the label and places the module on a storage rack. The light source will be twelve 1,000 Watt quart lamps with individual variac controls for each lamp. The light intensity will be set using 18 calibrated solar cells. Module measurements will be periodically checked with sunlight and Xenon flash simulator measurements to assure the correct calibration.

The module test subsystem components and the data flow are shown in Figure 32. The components are recommended based upon their use in similar test subsystems now in operation. The computer controlled testing will follow the flow chart overview shown in Figure 33.

Figure 32.

PANEL TEST SUBSYSTEM COMPONENT AND DATA FLOW

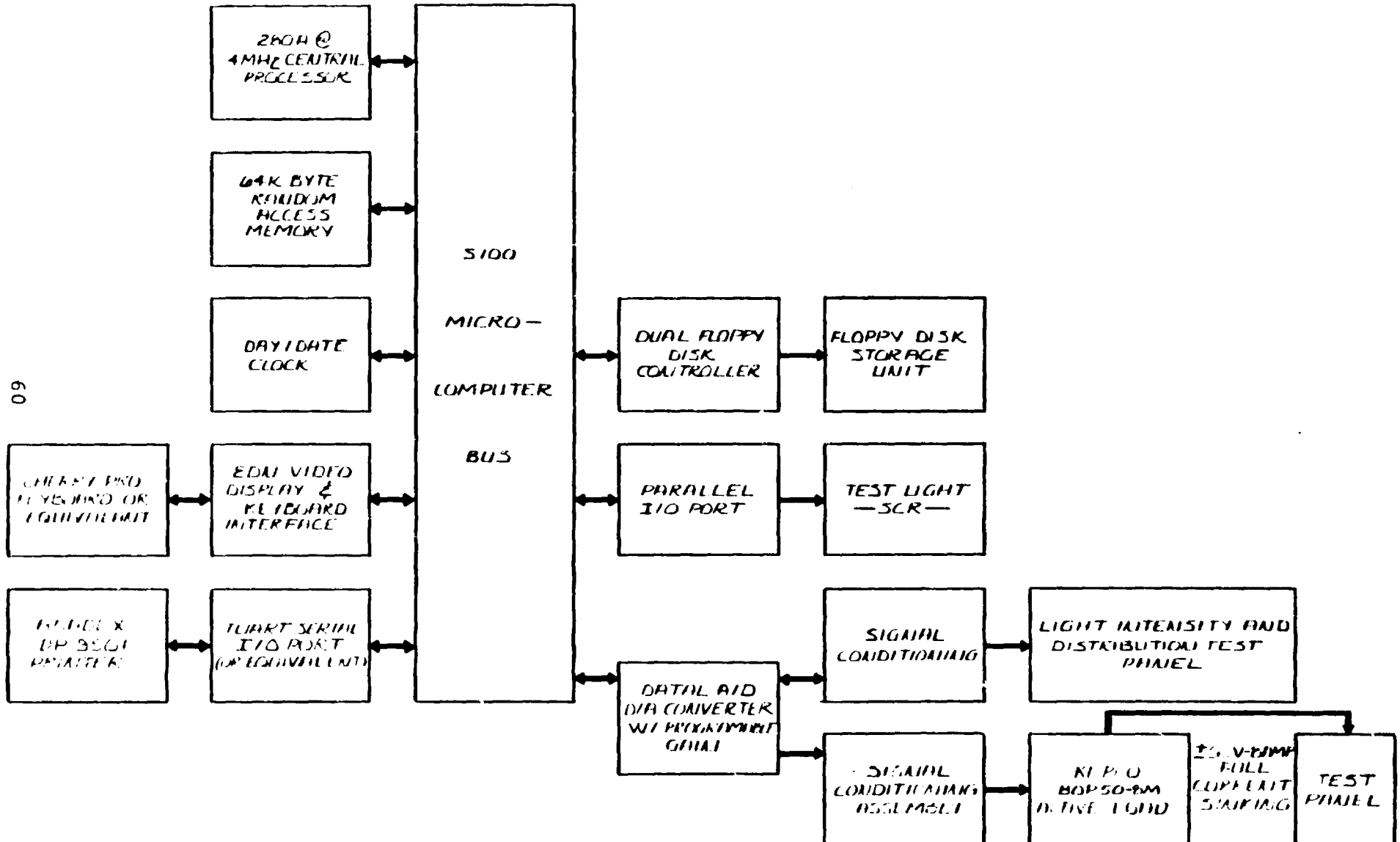
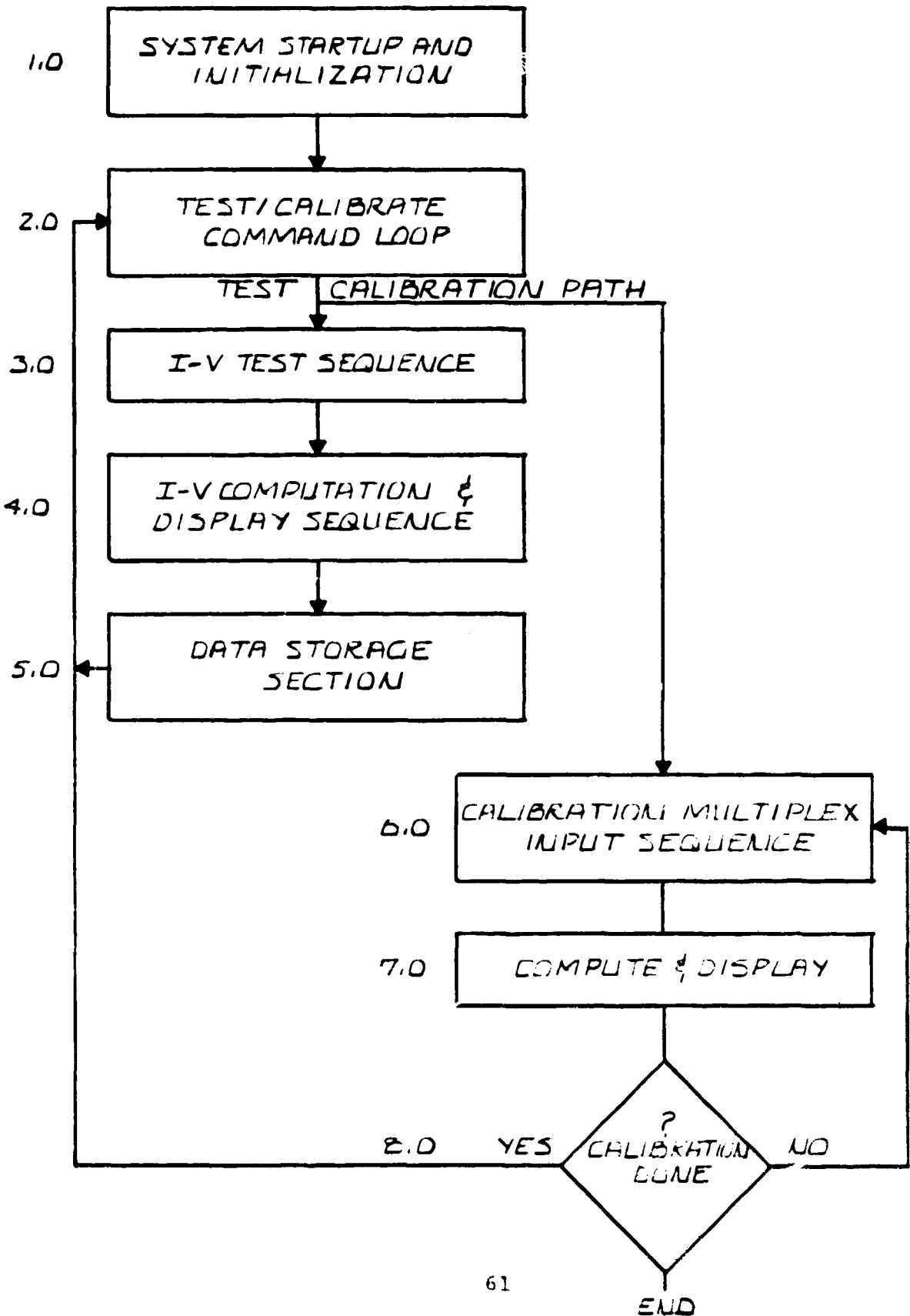


Figure 33.

# MODULE TEST OVERVIEW FLOWCHART



## 2.7 QA Plan

The preliminary MEPSDU QA Plan has been completed. It consists of the following documents:

- Quality Assurance Plan - MEPSDU QA 5000,
- Specifications for Semicrystalline Wafers Produced From Semix for MEPSDU - MEPSDU QA 5005,
- MEPSDU Incoming Inspection Procedure - MEPSDU QA 5003,
- In-Process Inspection Procedure - MEPSDU QA 5006,
- Test Procedure for the Measurement of Photovoltaic Cells - MEPSDU QA 5001,
- Cell Test System Functional Description - MEPSDU QA 5002,
- Module Test Procedure - MEPSDU QA 5007,
- Module Test System Functional Design - MEPSDU QA 5004.

It should be clearly noted that this is a QA Plan for the MEPSDU program, including the design development installation and technical readiness demonstration runs. It is not the QA Plan required for the production line that would result in 50 MW product to meet the \$0.70 per Watt cost goals.

Some important features of the QA Plan are given below.

In the area of equipment and materials, the QA Tasks are:

- Review equipment and materials specifications.
- Assess the effect of new technologies and use of alternate materials on performance.
- Interface with vendors to assure their capability to maintain quality standard required.
- Verify performance of equipment to determine reliability, maintainability and compliance with the specifications.

In the area of product fabrication, the QA tasks are as given below:

- Review manufacturing procedures and aid in determining the required controls.
- Establish incoming inspection procedures based on manufacturing requirements.
- Establish inspection criteria for in-process inspection.
- Develop process control stations.
- With manufacturing and engineering, determine the parameters to be monitored and what limits will be acceptable.

- Aid in development of the procedures required to collect the data required.
- Prepare control and information charts and a defect reporting system.

In the area of final tests, the QA tasks are as given below:

- Develop the cell test system.
- Develop the cell test procedure and perform required calibration tasks.
- Develop the module test system.
- Develop the module test procedure and perform the required calibration tasks.
- Perform measurements required to assure the reliability of the final cell and module test measurement.



## 2.8 Preliminary Cost Estimate

The preliminary cost estimates were performed, using the IPEG approximation. The results are shown in Table 1, along with the assumptions that the calculations are based on.

Table 1  
Price Estimates Using IPEG Approximation  
(1980 Dollars Per Watt)

Process	Cost Component				
	Equipment	Facility Space	Labor	Materials & Utilities	Total
Etch	.00046	.00024	.0008	.0006	.00746
Dry	.0003	.00026	.0018	.003	
Diffuse	.0046	.0014	.0043	.00337	.01367
Alloy	.0107	.00213	.0045	.0086	.0259
AR	.0021	.0011	.00505	.00104	.0093
Print	.005	.0028	.0074	.0016	.0168
Plate	.0007	.0005	.0045	.00806	.0219
Ink Off	.0003	.0033	.00372	.00083	
Solder	.0003	.00036	.00114	.0216	.0234
Laser	.00596	.0004	.0041	.0034	.0139
Cell QC	.004	.0019	.0118	.00086	.0186
String	.03026	.00413	.01112	.01724	.0628
Laminate	.0264	.0218	.0386	.0738	.1606
Module QC	.0012	.0023	.0056	.00162	.0107
Total	.09228	.04262	.10443	.14562	.385

Cell & Module  
Production      Wafers      Total Cost  
38.5      +    30.6¢      =    69.1¢

Assumptions: 15%-Efficient encapsulated cells  
93% total yield. Yield was not subtracted per step,  
but was subtracted at the end.  
50MW per year production rate

### 3.0 Technical Progress

The following section describes the technical effort during the first three months of the program.

#### 3.1 Documentation

The following documentation was submitted.

<u>Item</u>	<u>Submittal Date</u>
1. Baseline Cost Estimate	12/15/80
2. WBS	12/15/80
3. Draft Program Plan	12/23/80
4. Technical Progress Report No. 1	1/14/81
5. Technical Progress Report No. 2	2/13/81
6. Preliminary Design Review Package	2/26/81

#### 3.2 Kulicke and Soffa Industries, Inc. Subcontract

A Phase I design contract with Kulicke and Soffa was negotiated and approved. Kulicke and Soffa is to assist Solarex in designing the module interconnect scheme and is to design and provide a cost estimate for building a tabbing and stringing machine to perform the interconnection and module layout.

### 3.3 Surface Preparation

A preliminary process specification has been written based on our experience etching semicrystalline wafers. This specification will be utilized for subsequent cell fabrication. A preliminary design of an etching machine has been generated and discussed with several potential vendors. Preliminary sketches and requirements have been sent to these vendors. They are to provide us with recommendations and preliminary cost estimates.

### 3.4 Front Junction Formation

Spraying experiments at both Solarex, using a hand held air brush, and at Advanced Concepts, using an automated machine, were conducted. These experiments are described below.

(1) Emulsitone Phosphorofilm for Solar Cells was sprayed onto single crystal wafers using an air brush. The wafers were then baked at  $150^{\circ}\text{C}$  for 20 minutes. The dopant was diffused into the wafers in a quartz tube at  $850^{\circ}\text{C}$ . A matrix of experiments were conducted using (i) helium gas flow or (ii) no gas flow for either 5, 10 or 15 minutes. In all cases, the wafers developed an oxide which was extremely difficult to remove. Finally, steam oxide was regrown on the wafers and this enabled us to remove all of the oxide in dilute HF. Sheet resistances on the samples varied from 300 to 600 ohm/square.

Subsequent discussions with Emulsitone indicated that oxide removal could be facilitated by performing the diffusion in the presence of oxygen.

(2) The second experiment used the same starting material, spray technique and bake as before. However, this time the diffusion temperature was  $910^{\circ}\text{C}$  and oxygen was passed through the tube during the diffusion process. All wafers were diffused for 10 minutes. The diffusion oxides were

easily removed in dilute HF. Sheet resistances were tightly grouped between 40 and 60 ohm/square and were uniform across each wafer (despite the non-uniformity of manual spraying).

Cells were fabricated from these wafers. The cells were 2 cm. x 2 cm. using a standard space process (Ti/Pd/Ag) except for the diffusion. The average power of these cells, 69.3 mW, is exactly the same as the average obtained using the standard process in the Impurities Analysis Program, JPL Contract 955307. These results show the spray-on diffusion process can provide cells as good as those obtained by diffusion, with excellent consistency within the group.

(3) A solution of 10%  $\text{H}_3\text{PO}_4$  in ethanol was manually sprayed onto single crystal wafers. These cells were then coprocessed with No. 2 above. The sheet resistance varied from 10 to 55 ohm/square. The variation in sheet resistance across each wafer was considerably greater than was observed for the wafer sprayed with the Emulsitone dopant. Indeed, this solution did not wet the wafers as completely as the Emulsitone dopant did. Because of the initial success with the Emulsitone dopant, no further experiments with alternate formulations are contemplated.

(4) Single crystal wafers were prepared using the preliminary MEPSDU etch process sequence. These wafers were then shipped to Advanced Concepts Equipment Company for

spraying with the Emulsitone dopant. Six wafers each were sprayed under the following conditions:

- (i) 5cc/min - belt speed 18in/min - fine spray
- (ii) 5cc/min - belt speed 18in/min - medium spray
- (iii) 10cc/min - belt speed 18in/min - fine spray
- (iv) 10cc/min - belt speed 18in/min - medium spray

These wafers were baked at 150°C for 20 minutes at ADC and then shipped back to Solarex. They were then diffused as Nos. 2 and 3 above, 910°C for 10 minutes with oxygen flow. The diffusion glass was removed in dilute HF. The glass striped more easily from the 5cc/min samples than from the 10cc/min samples. The sheet resistances were:

- (i) 5cc/min - fine spray - 36 - 48 ohm/square
- (ii) 5cc/min - medium spray - 35 - 45 ohm/square
- (iii) 10cc/min - fine spray - 30 - 45 ohm/square
- (iv) 10cc/min - medium spray - 32 - 46 ohm/square

Semicrystalline silicon was processed into cells. Two groups were processed, using wafers from the same brick. One group received standard gaseous diffusion, while the second group was hand-sprayed with "Phosphorofilm for Solar Cells." The measured sheet resistivity was about 20 ohm/square for the standard diffusion wafers, and about 30 ohm/square for the spray-doped wafers. Both groups were then co-processed through standard methods (Ti/Pd/Ag) and the resulting cells

were tested at AMO and AM1. Each group contained 51 finished  
2 cm. x 2 cm. cells.

Group	Gas-diffused		Spray-doped	
	AMO	AM1	AMO	AM1
Power,mW (%eff.) Avg.	50.5(9.4%)	43.1(10.8%)	49.6(9.2%)	43.1(10.8%)
Voc,mV Avg.	567	559	549	545
Isc, mA Avg.	123	108	122	105

Summary of Cell Data



### 3.5 Back Junction Formation

A preliminary process sequence was written for the screen printing, drying and firing of the aluminum paste. Experiments were conducted to determine if an HCl etch or mechanical abrasion should be utilized to clean up the paste residue.

Samples cleaned up in a Fluoroware System, Inc. (FSI) spin/etch system using sprayed HCl were evaluated by measuring the infrared reflectance to determine the degree of cleanliness obtained. Cells that had been through the FSI system were measured for reflectance and transmittance in the IR. They were then recleaned using the standard HCL soak technique and then remeasured. There was no measurable change in the combined value of reflectance and transmittance, indicating no appreciable change in the condition of the back surface. Microscopic examination of the FSI cleaned wafers indicated cleaned backs with only a few brown or black particles.

Initial experiments were conducted to determine if sand blasting could be used to clean up the Al residue. After Al firing, the wafers were sprayed at 30 lbs. per sq. in. pressure using MDC super fine glass balls as the spray medium. The spraying was done by hand with little control over the amount removed except that the backs were shiny when complete. The samples were then nickel plated and the nickel did plate to the aluminum. Tabs were soldered to the back using solder

paste. The results of the pull tests varied from 0 to 7 oz. with a mean of about 2.5 oz. The metallization separated between the Ni and Al.

Single-crystal samples were prepared using processes similar to the proposed MEPSDU processes. After firing of the Al paste, they were sand blasted at a local commercial establishment using medium industrial grade glass beads. The paste residue was easily removed, leaving clean aluminum. Attempts were made to Ni plate the samples. With no subsequent treatments, the Ni would not plate to the Al. After cleaning in the HF fumes, as would be done during normal processing, the Ni did plate to the Al but all pull strengths were less than 10 oz.

In an attempt to improve the adhesion of Ni to Al, we have explored the use of a zinc immersion plating bath, a standard commercial pretreatment for Ni plating to Al. The bath is an aqueous solution of zinc oxide (84 g/l) and sodium hydroxide (402 g/l). The wafers were immersed for 10 sec. at room temperature, diluted in distilled water and then plated for seven minutes in Halma Ni solution at 85°C, pH 8.5. Tabs were soldered directly to the nickel. Pull strengths ranged from 10 oz. to 35 oz. with an average of 24 oz. However, in subsequent processing, the Zn immersion plating appeared to inhibit good Ni adhesion on the front of the cells. Work in this area is continuing.

### 3.6 AR Coating

Single crystal wafers were sprayed with the titanium isopropoxide AR solution using a hand spray gun. While we got a blue coating, it was uneven due to the lack of spraying control. Some of these samples were satisfactorily utilized in subsequent metallization experiments.

Single crystal and semicrystalline wafers were sprayed by Advanced Concepts with the titanium isopropoxide AR solution. Elipsometry measurements yielded an average film thickness of  $850 \text{ \AA}$  with a variation of approximately  $\pm 100 \text{ \AA}$ . The index of refraction varied from 2.1 to 2.2 with an average of 2.16.

### 3.7 Metallization

#### 3.7.1 Resist Inks

We have extended considerable efforts in identifying a resist ink that

- Can survive the AR coating etch.
- Can survive the Ni plating bath.
- Will not bleed into the areas to be plated.
- Can print well and be easily and quickly cured.
- Should be easily and completely removed.

The following resists have been evaluated:

- Warnow Printed Circuit Resist PR1000 - Appears to survive 30 sec. in fuming 70% HF but not 2 min. in 48% HF; not completely soluble in either toluene or trichloroethylene, requires a vapor degreaser.
- Hilton-Davis Sup-R-Cryl 5-54-A-300 - Too fluid for good printing; not completely soluble in either toluene or trichloroethylene.
- Chroma-Chem 844 - Too fluid for good printing.
- Inmont RBH - Prints well, dries extremely quickly; all wafers broke in plating bath.
- Universal Color Dispersions UCD 4800A - Excellent printing, no visible breakdown of resist in plating.

solution; does not completely dissolve in acetone or trichloroethylene.

- MacDermid Macu-Mask 9251 and 9454 - Good clear print; does not break down in plating solution; is completely removed by trichloroethylene (5 min. ultrasonic); 9251 was tested by  $\text{TiO}_x$  with etching by 1:1 HF - appears to be undercut; pattern areas are widened considerably.
- Homemade resists using solid Rhome and Hass Acryloids A-21, B-44, B-48N and B-50 mixed in ethylene glycol monobutyl ether acetate (Butyl Cellosolve) - Prints well; withstands HF etch; is undercut by the Ni plating solution.
- Homemade resist using solid Rhome and Hass Acryloids B66 + B82 and blue dye LCB 2005 mixed in Butyl Cellosolve - Prints well; withstands funic HF etch; is undercut by the Ni plating solution; at times can be stripped by cold water while at other times is very hard to remove.
- Colonial Printing Resist ER-6028 R.U. Blue - Prints well and cures in 3 to 6 mins.; survives best the etching and Ni plating of all the inks tested; is removable in cold organic solvents, although residue may be a problem.

To date, we have selected the Colonial Resist as our prime choice, with the Warnow as a back-up.

### 3.7.2 Etching of AR Coating

A variety of liquid HF solutions were studied and none satisfactorily removed the titanium oxide AR coating. It has now been determined that the titanium oxide AR coating can be etched in the vapors from room temperature 70% fuming HF. The wafers are placed in the vapors for 30 seconds to remove the AR coating layer without affecting the resist. Careful examination of the sample indicates that there are small isolated crystals of what appears to be metallic titanium left in the pattern. These small patches do not retard Ni plating nor do they effect contact resistance so their presence does not present a problem.

### 3.7.3 Tab Pull Tests

In order to evaluate the Ni-solder metallization proposed, a number of tab pull tests have been conducted. The initial pull tests showed significant scatter with low pull strength corresponding with stains on the silicon and low electrical performance of the cells.

Pull test experiments utilizing the MEPSDU laboratory processes with the Warnow resist ink as a function of plating time yielded the following results.

6 minutes	12.4 oz.	S.D. 8.7
6 minutes	11 oz.	S.D. 10
7 minutes	7.5 oz.	S.D. 4
9 minutes	2.7 oz.	

The results indicate that the plating time and, therefore, thicknesses are critical to achieve the required pull strength. We also believe that our liquid immersion of the wafers into the solvent does not remove all of the Wornow resist.

A set of cells using the Colonial Ink were processed and tab pull tests performed. The tabs were soldered using a 900°F soldering iron. The results of the tests are shown below:

0	-	3.5 oz.	14 tabs
3.5	-	7 oz.	13 tabs
7	-	14 oz.	12 tabs
14	-	21 oz.	9 tabs
21	-	28 oz.	10 tabs
greater than 28		oz.	6 tabs

During the test, it was noted that some of the failures occurred at the solder joint, not in the cell metallization. Further investigation indicated that a 900°F soldering iron may be too hot for soldering to Ni-solder metallized cells.

A second group of cells were prepared in the same way, but the tabs were soldered using a 600°F soldering iron. The results of the tab pull tests follow:

0 - 7 oz.	1 tab
7 - 14 oz.	2 tabs
14 - 21 oz.	5 tabs
21 - 28 oz.	6 tabs
28 - 35 oz.	12 tabs
greater than 35 oz.	14 tabs

Separation occurred at the Ni-Si interface with some silicon pulled away in most cases. These are exceedingly good results and they indicate the importance of fine control over the soldering process.

Experiments were also conducted to investigate the effect of lamination time-temperature cycles on the metallization. Cells were made using Ni-solder metalization and then tabbed. Half of the group was tab pull tested as is while the other half was heated at 150°C for one hour. If the cells were properly cleared before Ni plating, the pull strengths were either constant or were higher after the heat treatment, indicating that this metallization is compatible with the laminating process.



### 3.8 Edging

Discussions were held with laser scribe manufacturers, particularly Quantrad about the use of their system with 10 cm. x 10 cm. semicrystalline silicon solar cells. Their system can scribe any preprogrammed shape on any object positioned under the laser. The scribe must be programmed to scribe inside of the smallest size cell that will be processed. Therefore, a significant function of the active area may be lost for larger cells. Two ways around this problem are:

- To place a tight tolerance on cell size so that not much active area is lost, or
- Use an edge follower system that scribes a prescribed distance inside the edge of the wafer, not a fixed pattern system.

Preliminary discussions with manufacturers indicate that such an edge following system is feasible for MEPSDU.

### 3.9 Cell Design

The front cell pattern was designed. The analysis was based on the following information:

- Four pads are located on two opposite edges of the cell (see Figure 34).
- N+ layer sheet resistance =  $40 \Omega/\square$ .
- Minimum controllable bus width is 18 mils.  
(We will try to reduce this during the course of the program.)
- Solder is flat across the top, indicating an almost rectangular cross section.
- Resistivity of the solder =  $20 \cdot 10^{-6} \Omega \cdot \text{cm}$
- Relationship between initial base width and height of solder was measured as shown below:

Initial Bus Width	Width of Solder	Height of Solder
<u>(MIL)</u>	<u>(MIL)</u>	<u>(MIL)</u>
18	18	3
60	60	6
100	100	9

APPLICATION		REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED
			<p>MAX. 10.03CM. OR 3.949"</p> <p>NOM. 10.00CM. OR 3.937"</p> <p>MIN. 9.97CM. OR 3.925"</p> <p>9.913CM. OR 3.903"</p> <p>9.075CM. OR 3.573"</p>		
			<p>.381CM. OR .15"</p> <p>.051CM. OR .032"</p>		
			<p>7.310CM. OR 2.878"</p> <p>.381CM. OR .15"</p> <p>2.330CM. OR .909"</p>		
			<p>.381CM. OR .15"</p>		
			<p>9.919CM. OR 3.905"</p> <p>MAX. 10.03CM. OR 3.949"</p> <p>NOM. 10.00CM. OR 3.937"</p> <p>MIN. 9.97CM. OR 3.925"</p>		
			<p>.381CM. OR .15"</p>		
			<p>3.18CM. OR .125"</p> <p>LASER SCRIBE LINE .001" WIDE-.003" DEEP</p> <p>MAX. .318CM. OR .125"</p> <p>MIN. .238CM. OR .094"</p>		

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±		CONTRACT NO.		<div style="text-align: center;"> <b>SOLAREX CORPORATION</b>          1335 PICCARD DRIVE ROCKVILLE, MD 20850 □ 301 948 0202       </div>
		APPROVALS	DATE	
MATERIAL	DRAWN	2-19-8	MEPSDU CELL OUTLINE & PACE PLACEMENT	
	CHECKED	2-18-8		
FINISH				
DO NOT SCALE DRAWING		SIZE <b>A</b>	CODE IDENT NO. Figure 34	DRAWING NO. <b>1006</b>
		SCALE		SHEET 1 OF 1

- Ignore contact resistance since we do not know the value for  $N_i$  and because previous calculations that have ignored the term have agreed well with actual cell performance.

The technique for determining the pattern entails defining all of the power loss terms and then minimizing the total power loss with respect to grid spacing and bus width. The grid width is assumed to be the minimum allowable by technology since using the minimum line width always yields the smallest power loss.

For the grid lines there are three power loss terms:

1) Shadowing

$$\Delta P_s = \text{Area of Grids} \cdot P$$

2) Sheet Resistance In Diffused Region

$$\Delta P_D = \frac{J^2 R X^2 A_n}{12}$$

3) Loss In Grid Lines

$$\Delta P_G = \frac{J^2 X L^2 P_s A_n}{3aT}$$

Where  $P$  = Power Density Produced by Si  
under 1  $\text{Sun}$  illumination  $\approx$   
 $0.015 \text{ W/cm}^2$

$$\text{Area of Grids} = \text{Area of Each Grid} \cdot \frac{\text{Length of Cell}}{X}$$

$X$  = Spacing between grid lines

$R$  = Sheet resistance =  $40 \Omega/\square$

J = Current density produced by Si  
under 1 Sun Illumination  $\approx 0.03 \text{ A/cm}^2$

A = Area collected by each grid

N = Number of such grid region

AN  $\approx$  Area of cell =  $10 \text{ cm}^2$

L = Length of grid line

Ps = Resistivity of solder =  $20 \cdot 10^{-6} \Omega \text{ cm}$

O = Width of grid line

T = Thickness of grid line

The only unknown is X, grid spacing

Total power loss due to grid lines is given by:

$$\Delta P_T = \Delta P_S + \Delta P_D + \Delta P_G$$

Minimize power loss with respect to spacing

$$\frac{d\Delta P_T}{dx} = 0$$

Solve for X.

Results: X = 0.475 cm (187 MILS)

$$\Delta P_S = 0.139 \text{ W}$$

$$\Delta P_D = 0.068 \text{ W}$$

$$\Delta P_G = 0.005 \text{ W}$$

$$\Delta P_T = 0.212 \text{ W}$$

In calculating the bus bar width, we did not use a tapered bus because the form of the equations are extremely complicated (compounded by the fact that the thickness is a function of the width). The calculations were performed for a stepped bus and approximated by the closest taper. For the bus, the two power loss terms are:

1) Shadowing

$$\Delta P_S = \text{Area of bus} \cdot P$$

2) Resistance in Bus

$$\Delta P_M = (JA)^2 \frac{\rho s L}{YT}$$

where A = Area collect from

L = Length of each region of stepped bus

Y = Width of bus in each region

T = Thickness of bus in each region

Total power loss due to each bus bar region:

$$\Delta P_T = \Delta P_S + \Delta P_M$$

Minimize the power loss with respect to the bus bar width in each region.

$$\frac{d\Delta P_T}{dy} = 0$$

The results are given in the following table.

<u>Segment Number</u>	<u>Optimized Width (cm)</u>
1	0.048
2	0.048
3	0.068
4	0.088
5	0.104
6	0.120
7	0.136
8	0.152
9	0.167

We have used a taper from 0.05 cm to 0.178 cm. With this value, the power losses for all four bus bars in the cell are given by:

$$\Delta P_S = 0.032 \text{ W}$$

$$\Delta P_M = 0.084 \text{ W}$$

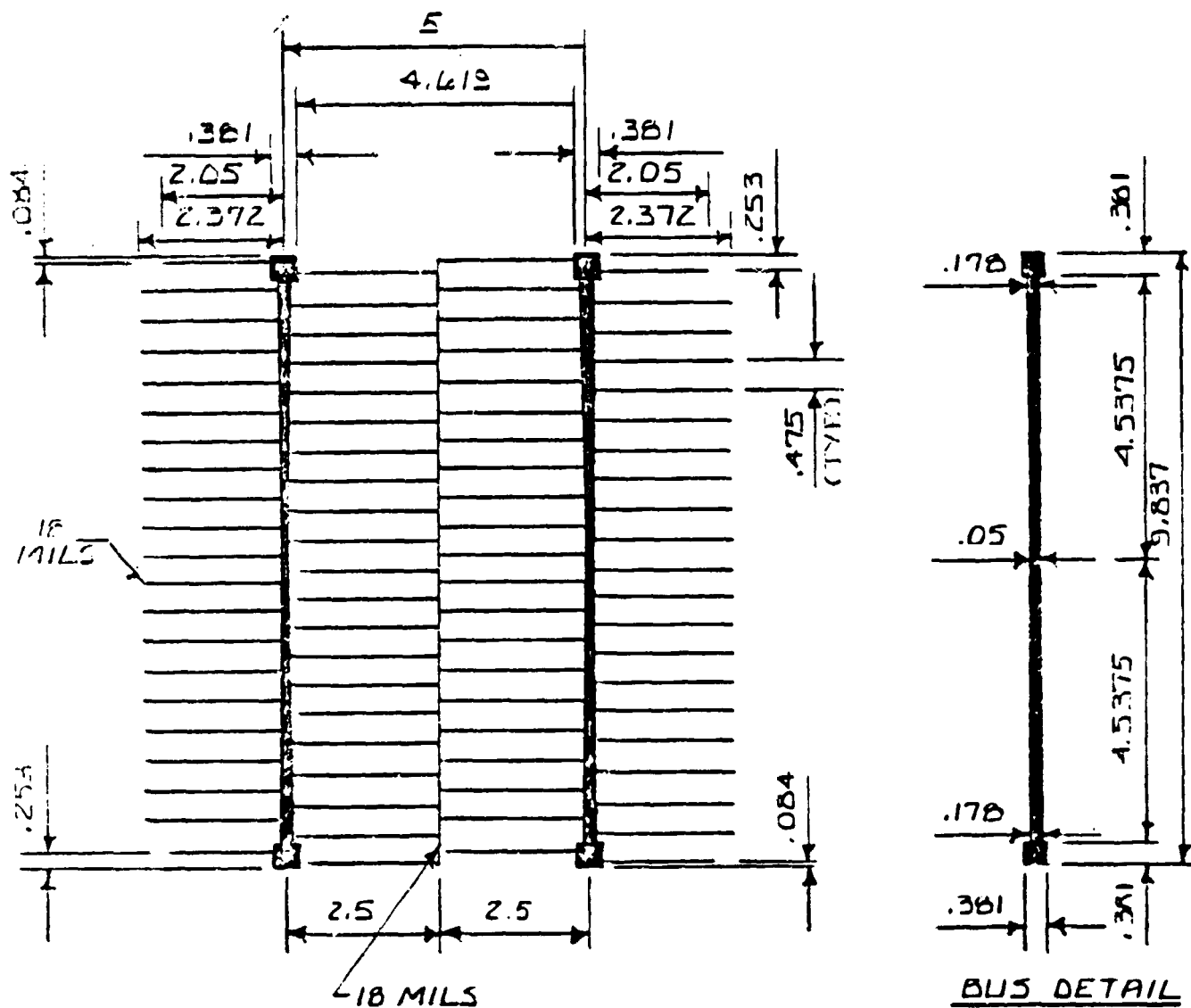
$$\Delta P_T = 0.116 \text{ W}$$

The final power loss term comes from shadowing of the pads. This contributes a power loss of

$$\Delta P_{\text{pad}} = 0.009 \text{ W}$$

The cell pattern is shown in Figure 35. The total area covered by the grid is  $12 \text{ cm}^2$ , while all of the power loss associated with N side collection is  $\Delta P_T = 0.337 \text{ W}$ .

APPLICATION			REVISION			
NEXT ASSY	USED ON	LTR	DESCRIPTION	DATE	APPROVED	



NOTE:  
ALL DIMENSIONS IN CM.  
UNLESS MARKED OTHERWISE

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± XXX ±	CONTRACT NO.		<b>SOLAREX CORPORATION</b> 1335 PICCARD DRIVE ROCKVILLE, MD 20850 □ 301 948 0202		
	APPROVALS	DATE			
	MATERIAL	DRAWN <i>J. K. 107</i>	2-23-81	MEPSDU 10 CM. X 10 CM. GRID PATTERN	
	FINISH	CHECKED <i>[Signature]</i>	2-24-81		
DO NOT SCALE DRAWING	SCALE		SIZE <b>A</b>	CODE IDENT NO. Figure 35	DRAWING NO. <b>1008</b>
SHEET			1 OF 1		



### 3.10 Module Design

The preliminary mechanical and electrical design of the module was complete. A drawing package was completed for the Preliminary Design Review. This package included the following drawings:

- MEPSDU Top Assembly 1 of 2 and 2 of 2 (see Figure 36),
- MEPSDU Cell Assembly 1 of 2 and 2 of 2 (see Figures 8 & 37),
- MEPSDU Cell Outline and Pad Placement,
- MEPSDU 10 cm. x 10 cm. Grid Pattern,
- MEPSDU Interconnect,
- MEPSDU Gasket,
- Identification Label,
- MEPSDU Electrical Schematic (see Figure 38),
- MEPSDU Interface Control.

As part of the module design effort, we reviewed the interconnect design with K&S and with several vendors. An experimental quantity of interconnects have now been ordered from Wyngard & Co.

Discussions have also been held with Varo, a diode manufacturer, about the possibility of them supplying an integrated buss bar-diode package for incorporation in the MEPSDU module.

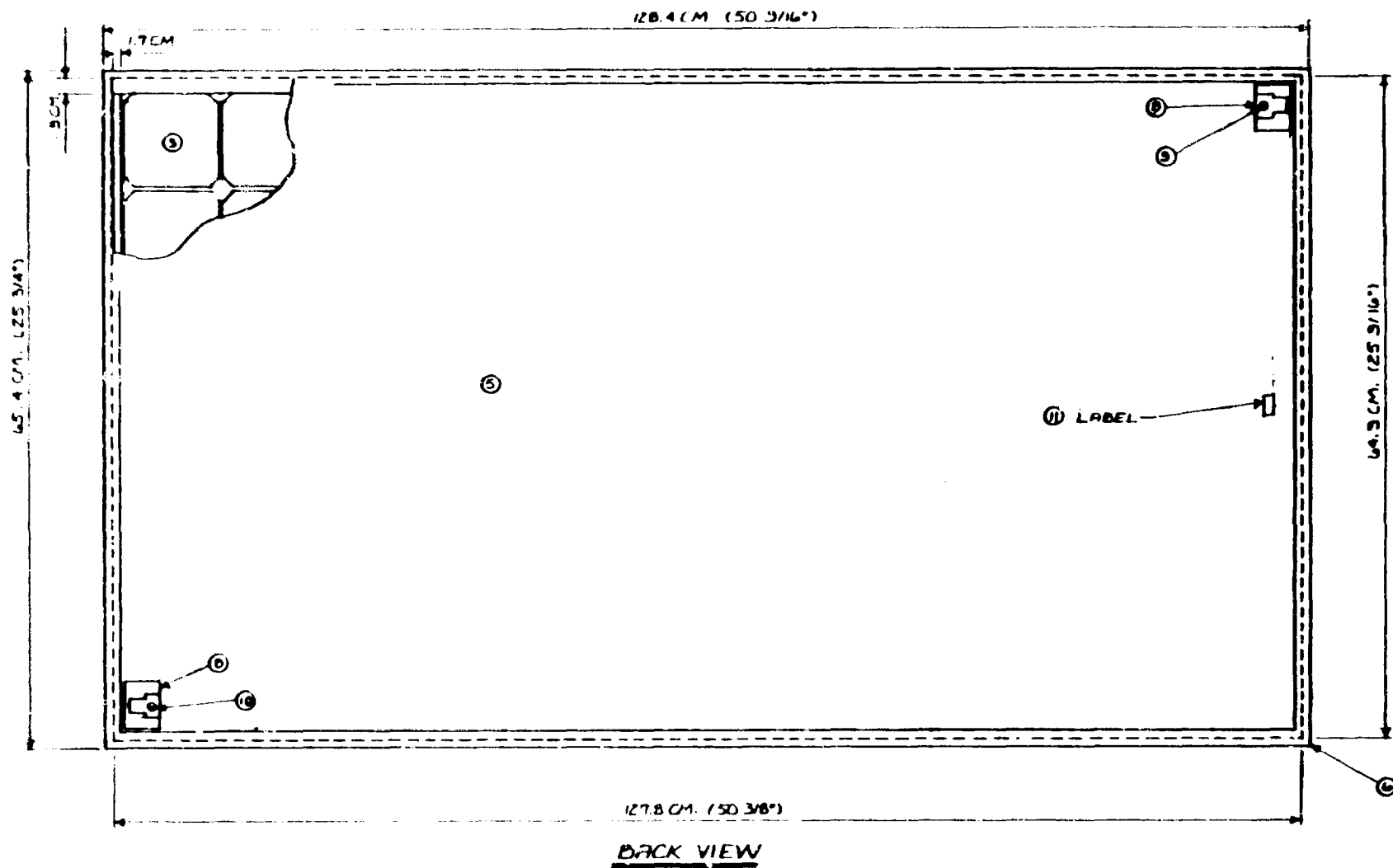
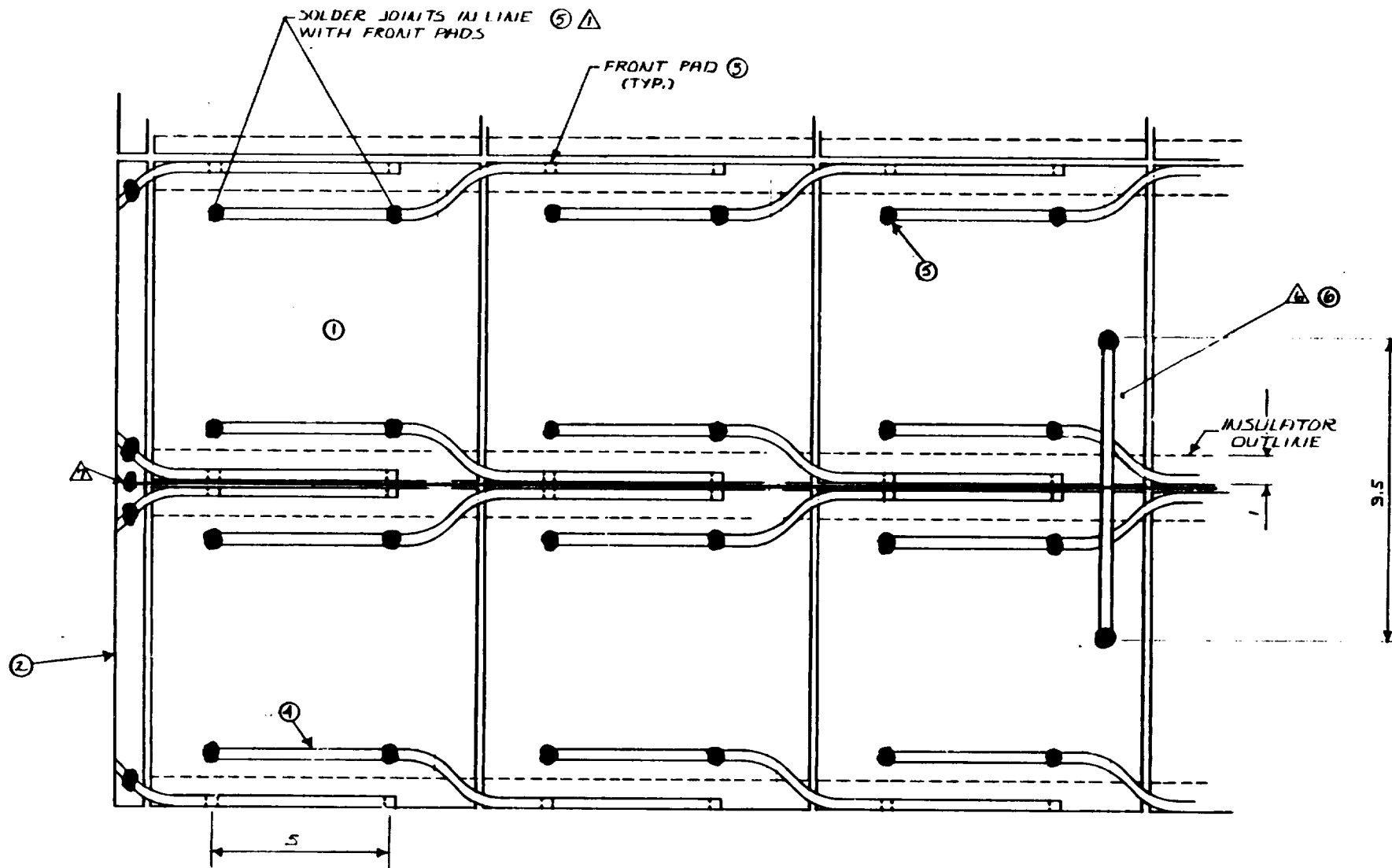


Figure 36. MEPSDU Top Assembly

2-2

91



DETAIL "A"  
FULL SIZE

Figure 37. MEPSDU  
Cell Assembly

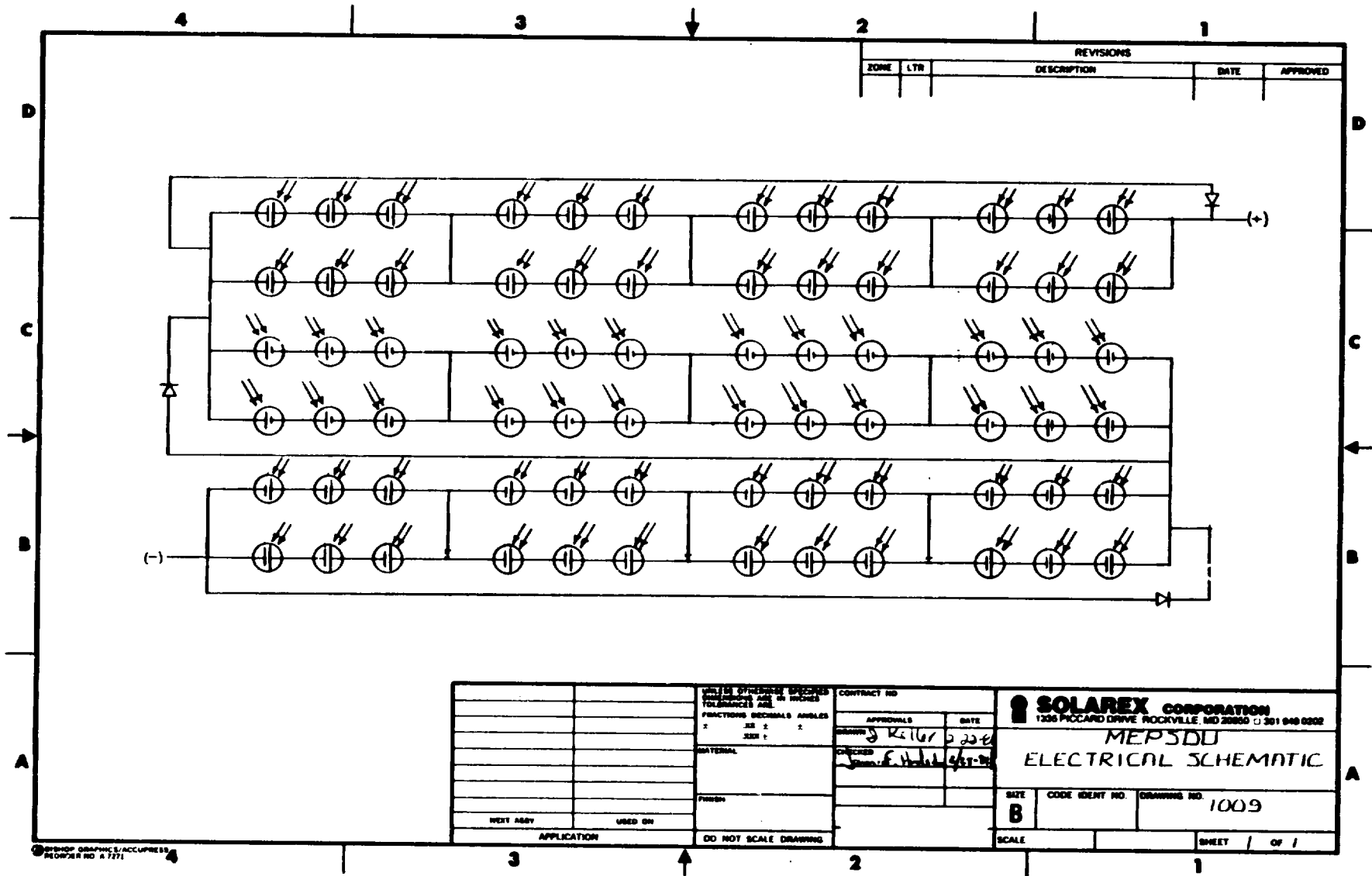


Figure 38. MEPSDU  
Electrical Schematic

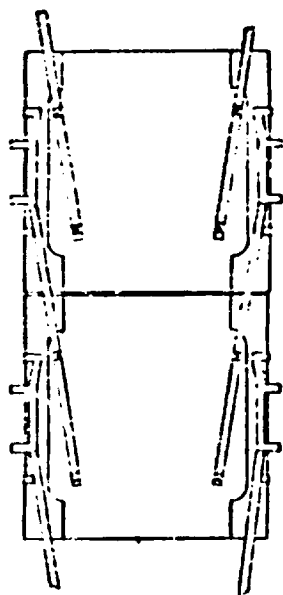
### 3.11 Tapping and Stringing Machine

As an alternative to the module design from the proposal, we investigated the use of a low cost wraparound design for added reliability and improved module performance.

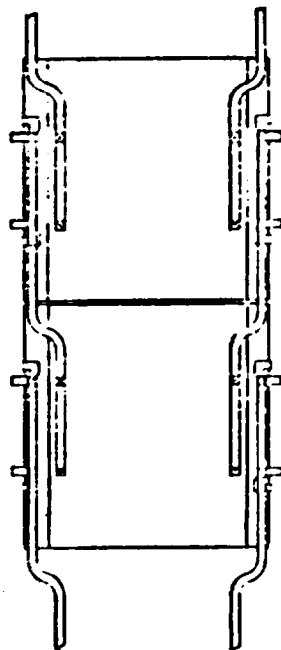
The 10 cm. square solar cell to be used in this project will have a metallization pattern with two (2) interconnect pads on each side of the cell. The basic approach is to bond an interconnect to each side of the cell, wrap the interconnect around to the back side of the cell, and then make the series connection to other cells in the same string and parallel connections to other strings, all from the back side.

During this period, Solarex and K&S concentrated on developing a cost effective interconnect system. Several interconnect configurations were studied, ranging from straight ribbon applied in a chevron manner to various designs of interconnects with projecting fingers which could be made by a punch and die technique within the machine or applied in a preform manner. Formed wire interconnect was also studied. Several of the interconnect configurations studied are shown in Figure 39.

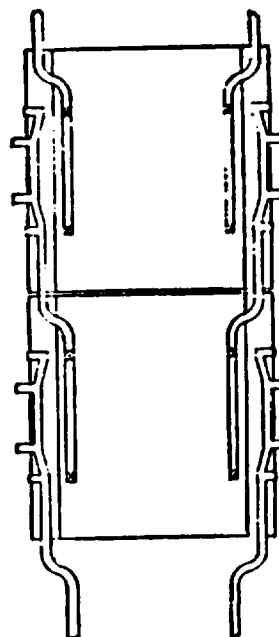
Another interconnect considered used a straight ribbon foil and tabs. In this concept, the insulation of the cell would be part of the machine cycle. Overall complexity and cost would be higher, but material costs would be reduced.



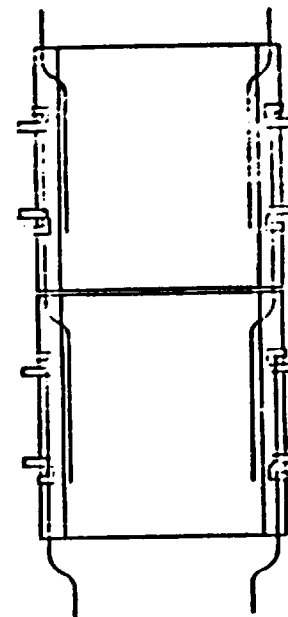
1. TAB STAMPING  
& RIBBON  
(PRE-INSULATED CELL)



2. 3\"/>



3. 3\"/>



4. 3\"/>

Figure 39. Interconnect Configurations

Many of these interconnect and insulating systems were modelled for evaluation purposes. Each interconnect configuration was evaluated from various viewpoints, such as:

- Number of bonds per cell,
- Number of bonds per module, including parallel connections,
- Estimated interconnect material costs (plain copper and solder coated copper),
- Number of machine functions required,
- Relative complexity and cost of machine required.

Several of the more promising interconnect configurations were further studied by K&S by means of a diagrammatic approach to the machine flow required to accomplish the desired system. This was done to get a relative idea of the complexity and cost of the machine to accomplish the tasks required for each system.

These studies of the interconnect configurations narrowed the selection down to the following candidates:

- One piece stamping,
- Nested ribbon, with or without J-strap wrap-around contact,

- Straight ribbon foil and tabs.

As a result of the comparison between the three interconnect configurations, and inputs from reputable die makers (who gave us not only some cost estimates, but some strong recommendations), the following preliminary design decision was made to proceed with the one piece stamping interconnect configuration, which combines the wrap-around contact and the series interconnection between the cells of the same string. Figure 11 showed this interconnect. Figure 37 shows how the cells will be connected using this interconnect.



### 3.12 Module Encapsulation

Efforts in the encapsulation area have centered around identification of a mechanical/vapor barrier and analysis of EVA cure properties.

#### 3.12.1 Vapor Barrier

Our prime candidate for a vapor barrier is polyethylene. Low density polyethylene film produced by blow molding has the toughness and puncture resistance required for the mechanical barrier. A data sheet is attached as Figure 40. The following table compares polyethylene with TEDLAR for dielectric strength and permeability of water vapor.

Material	Permeability to water vapor gr-mil/100 sq in/24 hr at 37.8°C	Dielectric* Strength Volts/mil
TEDLAR	3.2	3500
Low Density Polyethylene	1.0	500

\*This is for actual commercial films not pure material

There is a significant amount of long term experience with polyethelyne in an outdoor environment with sufficient data to indicate that black polyethylene has at least a 30 year lifetime in outdoor use. Using 6 mil thick polyethylene would cost 1/12th of the cost of 4 mil TEDLAR per panel.

Figure 40.

# DOWLEX Resin 2045

Linear Low Density Polyethylene



## For Blown Film Extrusion

**Melt Index: 1.0    Density: 0.920****Description:** Excellent Tear Strength, Outstanding Toughness and Puncture Resistance**Warning:** This material does not presently comply with FDA regulation 177.1520. A petition for compliance has been approved, but is not yet published in the Federal Register.**Fabrication Conditions for Tubular Film Extrusion:**

Melt Temperature = 450-500°F  
 Blow-up Ratio = 2:1  
 Optimum Gauge Range = 0.5-3.0 mil

Physical Properties <sup>1,2</sup>	ASTM Method	Value
Melt Index, gm/10 min .....	D-1238	1.0
Density, gm/cc .....	D-792	0.920
Vicat Softening Point, °C .....	D-1525	100
Tensile Yield, <sup>3</sup> psi .....	D-638	1800
Ultimate Tensile, <sup>3</sup> psi .....	D-638	3500
Ultimate Elongation, <sup>3</sup> % .....	D-638	1100
Tensile Modulus, <sup>3</sup> 2% Secant, <sup>2</sup> psi .....	D-638	40,000
<b>Film Properties<sup>1</sup> @ 1.5 mil</b>		
Dart Impact, gm .....	D-1709	250
Elmendorf Tear Strength, gm .....	D-1922	450
CD .....	D-1922	680
Tensile Yield <sup>3</sup> , psi .....	D-882	1500
CD .....	D-882	1600
Ultimate Tensile, <sup>3</sup> psi .....	D-882	5000
CD .....	D-882	4500
Ultimate Elongation, <sup>3</sup> % .....	D-882	750
CD .....	D-882	750
Gloss, 45° .....	D-2457	37
Haze, % .....	D-1003	16

<sup>1</sup>Typical properties; not to be construed as specification limits.<sup>2</sup>Compression molded samples.<sup>3</sup>Crosshead speed — 20 in/min

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† See "Safety Considerations" reverse side

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A number of four cell test modules have been fabricated using polyethylene and are now undergoing environmental testing.

### 3.12.2 EVA Cure Properties

Studies of EVA are geared toward providing an incoming material test and a technique for determining the degree of cure of the finished module.

Samples of EVA were provided to Monsanto to perform an oscillating disc Rheometer (ODR) test. The results at two different temperatures are shown in Figure 41 and 42. At 140°C, the time to 90% cure is 192.5 minutes. Indeed, even to effect a 60% cure requires 37.5 minutes while a 75% cure requires 96 minutes.

We have investigated four techniques for evaluating the degree of cure of EVA samples.

(1) Hardness Tests - Samples of EVA were measured by the Shore A hardness test (ASTMD2240) both before and after cure. The results are shown below.

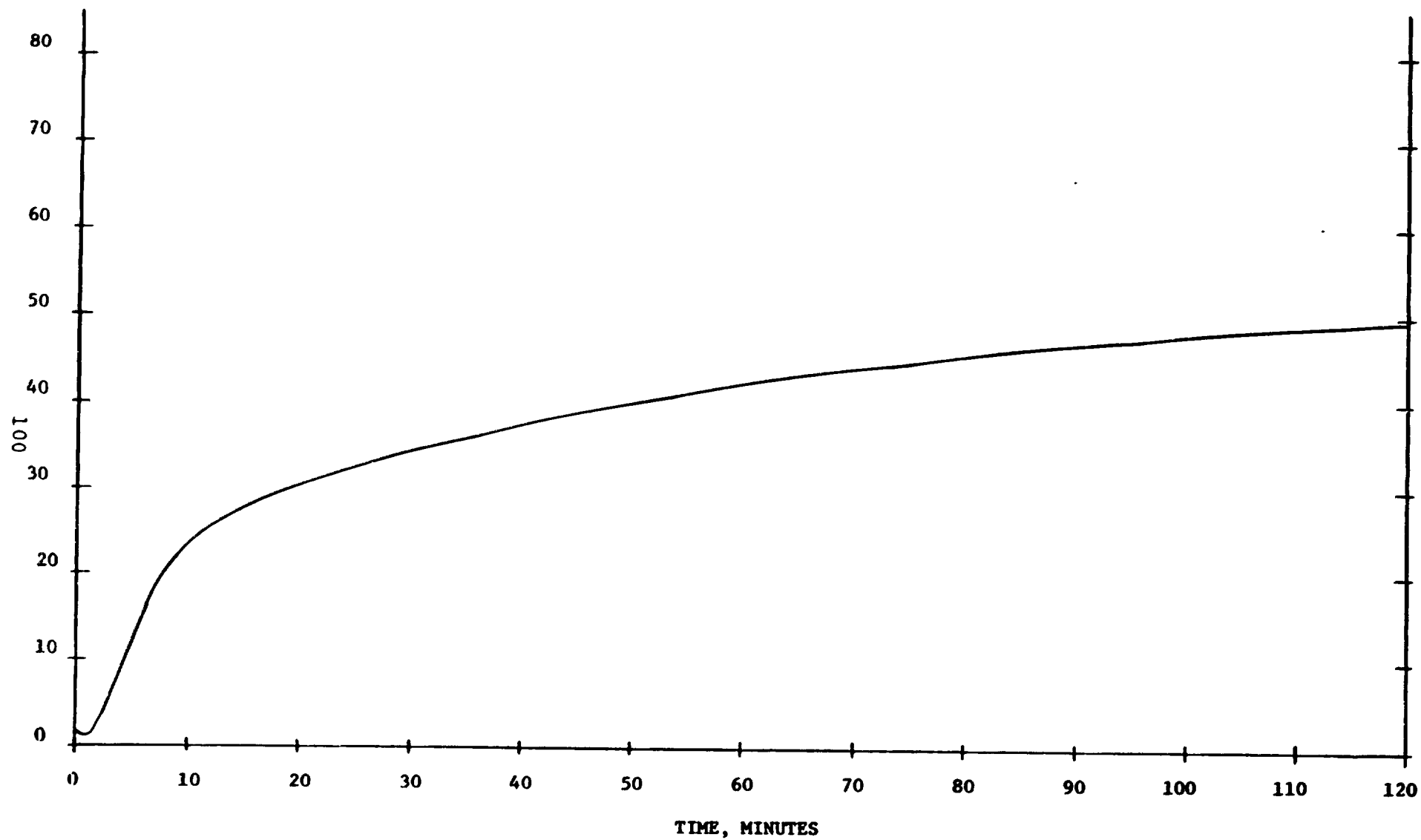


Figure 41. ODR Test at 150°C

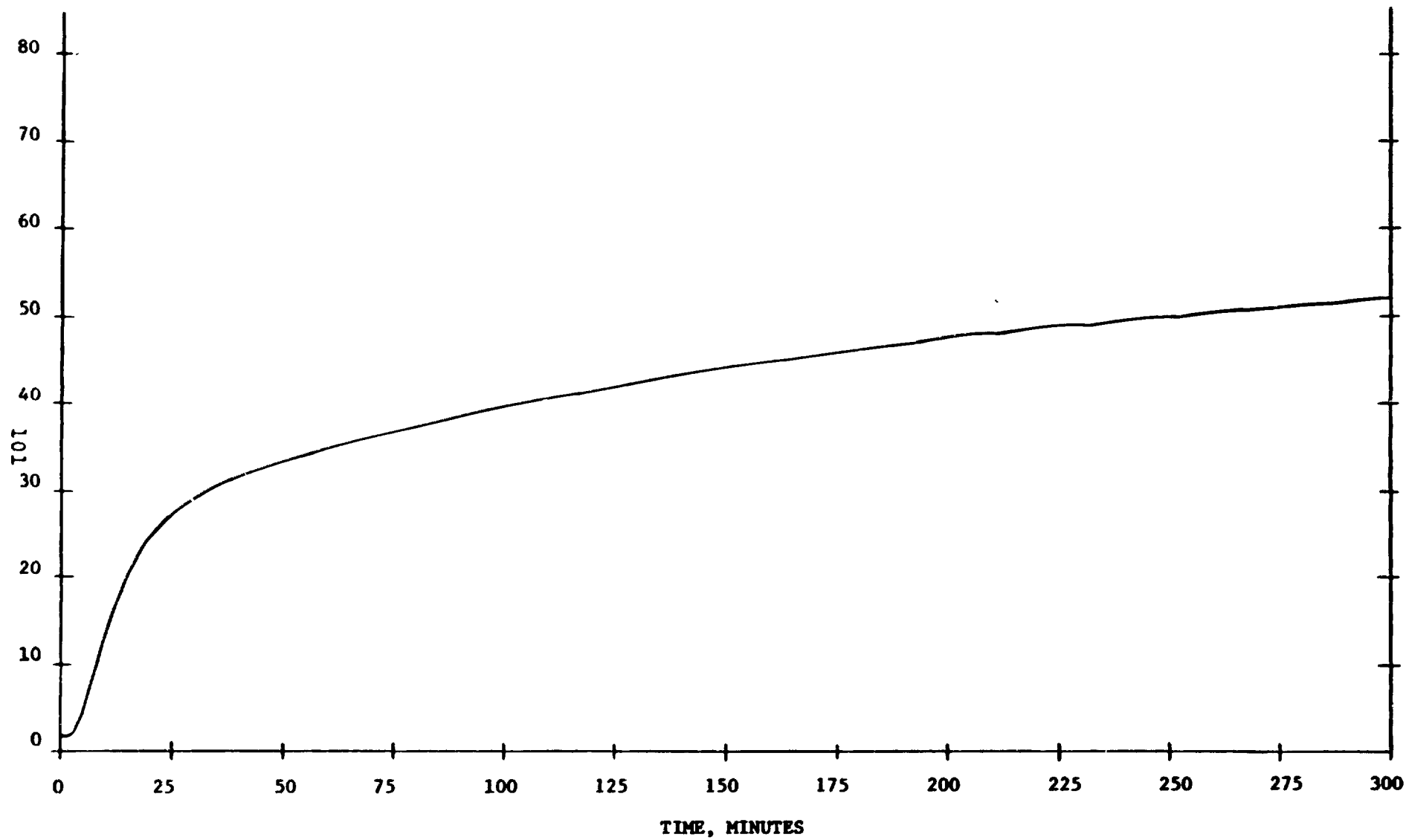


Figure 42. ODR Test at 140°C

## HARDNESS MEASUREMENTS

<u>Material</u>	<u>Shore A (ASTMD2240)</u>
Elvax 150, unmodified Dupont Lit. value	73
Elvax 150, unmodified remelted slab	69
Molded button Springborn sheet converted by JPL compression cure, 30 minutes	72
JPL molded button post cured 2 1/2 hours	72

It is apparent that the hardness value does not change significantly during the cure process and therefore can not be used as correlation for degree of cure.

(2) Gel Fraction - Gel fraction tests similar to those suggested by Springborn have been attempted. Preliminary results indicate that there is an observable difference between the resultant gel and the cure time at 138°C as shown below.

<u>Temperature</u>	<u>Cure Time</u>	<u>Type of Gel</u>
138°C	30 min.	very loose, light gel
138°C	1 hr.	moderate gel
138°C	3 hr.	fairly tight gel

It is apparent that very little curing occurs in the first thirty minutes.

(3) Gas Chromatography - Gas chromatography can be utilized to identify the amount of residual peroxide remaining in the sample. Accessory equipment for use in gas chromatography has arrived and experiments will begin soon.

(4) Creep Tests - Creep tests are now being utilized in conjunction with gel fraction tests to determine the appropriate cure cycle. Samples have been laminated using two pieces of glass with 23 layers of 15 mil EVA between them. These samples were then cured for a variety of times at 140°C. The samples are then placed vertically in an oven at either 70°C or 95°C. After 65 hours at 70°C:

- (i) A laminated, but not post cured, sample showed several inches of motion.
- (ii) A sample cured at 140°C for 30 minutes showed measurable but moderate motion (a fraction of an inch).
- (iii) A sample cured at 140°C for one hour showed no measurable creep.

After 65 hours at 95°C:

- (i) A sample cured for 30 minutes at 140°C showed measurable but moderate motion (a fraction of an inch).

- (ii) A sample cured at  $140^{\circ}\text{C}$  for one hour showed no measurable creep.

These tests are continuing to determine the long time behavior of these samples at elevated temperatures.



#### 4.0 Recommendation and Schedule

The following technical questions must still be answered:

- To develop a technique for removing all of the resist ink from the wafer,
- To prove that the sandblasting technique can yield an adequate pull strength or to develop a technique for limiting the solder on the back of the cell after HCL clean-up,
- What glass can meet the structural requirements,
- Whether the proposed lamination procedure is chemically compatible with the Springborn EVA formulation.

The following efforts will be undertaken during the next program period:

- Presentation of the Preliminary Design Review,
- Continued evaluation of the spray-on dopant on polycrystalline silicon,
- Evaluation of the FSI etching system,
- Evaluation of AR coating samples on polycrystalline silicon,

- Study of the Colonial resist with emphasis on clean-up and pull strengths,
- Continuation of the EVA cure tests,
- Evaluation of environmental testing of module and cells,
- Fabrication of cells using the MEPSDU process sequence,
- Identification of the MEPSDU equipment and suppliers,
- Submission, evaluation and start of K&S Phase II effort,
- Collecting data for preliminary SAMICS analysis.

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